

**FACULTY OF ENGINEERING**

# **Savitribai Phule Pune University**

**Syllabus for the**

**M.E (Electronics & Telecommunications Engineering –  
VLSI and Embedded Systems)**

**(2017 Course)**

**(w.e.f. June 2017)**

## Objectives

- I. To serve the University, the Nation, and the Engineering profession by providing high quality educational programs to all students; engaging in research and scholarship that will extend knowledge; and assisting the economic development of the regional, state, and national economies through technology transfer.
- II. To provide Post-graduate students with an excellent education through research and co-operative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.
- III. To sculpture Post-graduates students, to acquire the advanced level academic expertise and practical engineering experience necessary to function as Electronics and Telecommunication professional in a modern, ever-evolving world. Engrave Post-graduate students, to demonstrate competence by being selected for employment by industrial, academic or government entities or pursue further professional/doctoral studies.
- IV. To understand the broad, social, ethical and professional issues of contemporary engineering practice. Post-graduation program will inculcate a mastery of underlying Electronics and Telecommunication Engineering and related technologies, as well as professional, ethical, and societal responsibilities.

## Outcomes

- a) Masters students of this program have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.
- b) Post graduate students gain an ability to design and conduct experiments, as well as to analyze and interpret data.
- c) Learners of this program built an ability to design a system, component, devices, or process to meet desired needs.
- d) Masters students of this program have an ability to function on multi-disciplinary teams and also as an individual for solving issues of Electronics and Telecommunication.
- e) Learners of this program have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of Electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.
- f) Post graduates have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.
- g) Develop an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.
- h) Learners of this program have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, user friendliness etc. to cater needs for product development.
- i) Igniting master's students to peruse inventive concept to provide solutions to industrial, social or nation problem.
- j) Masters of this program generate an ability to identify, inspect, analyze, interpret and communicate research results.
- k) Post graduates recognize the need and an ability to engage in life-long learning and knowledge of contemporary issues.
- l) Masters of this program put on the broad education necessary to understand the impact of Electronics and Telecommunication solutions in a global, economic, environmental, and societal prospective.

## **Syllabus Details**

**M.E. (Electronics and Telecommunications-  
VLSI and Embedded Systems)**

**2017 Pattern  
Syllabus Structure**

**First Year – Semester I**

Sr.No.	Subject Code	Subject	Examination Scheme					Credits	
			L/P	Paper		TW	OR		Total
				ISA	ESA				
1	504201	Digital CMOS Design	4	50	50	-	-	100	4
2	504202	Reconfigurable Computing	4	50	50	-	-	100	4
3	504203	Embedded System Design	4	50	50	-	-	100	4
4	504204	Research Methodology	4	50	50	-	-	100	4
5	504205	Elective I	5	50	50	-	-	100	5
6	504206	Lab. Practice I	4	-	-	50	50	100	4
		<b>Total</b>	<b>25</b>	<b>250</b>	<b>250</b>	<b>50</b>	<b>50</b>	<b>600</b>	<b>25</b>

**Elective I:**

1. Micro Electromechanical Systems
2. Nano Technology
3. Processor Design
4. Wireless Sensor Networks
5. MOS Device Modeling and Characterization

## First Year – Semester II

Sr.No.	Subject Code	Subject	Examination Scheme					Credits	
			Paper						Total
			L/P	ISA	ESA	TW	OR		
1	504207	Analog CMOS Design	4	50	50	-	-	100	4
2	504208	System on Chip	4	50	50	-	-	100	4
3	504209	Embedded Automotive Systems	4	50	50	-	-	100	4
4	504210	Elective II	5	50	50	-	-	100	5
5	504211	Lab. Practice II	4	--	---	50	50	100	4
6	504212	Seminar I	4	-	-	50	50	100	4
		<b>Total</b>	<b>25</b>	<b>200</b>	<b>200</b>	<b>100</b>	<b>100</b>	<b>600</b>	<b>25</b>

### Elective II :

1. Embedded Product Design
2. High Speed ICs
3. Mixed Signal IC Design
4. Embedded Signal Processor Architectures
5. Real Time Operating Systems

## Second Year – Semester I

Sr.No.	Subject Code	Subject	Examination Scheme					Total	Credits
			Paper						
			L/P	ISA	ESA	TW	OR		
1	604201	Testing and Verification ofVLSI Circuits	4	50	50	-	-	100	4
2	604202	ASIC Design	4	50	50	-	-	100	4
3	604203	Elective III	5	50	50	-	-	100	5
4	604204	Seminar II	4	--	----	50	50	100	4
5	604205	Project Stage I	8	--	---	50	50	100	8
		<b>Total</b>	<b>25</b>	<b>150</b>	<b>150</b>	<b>100</b>	<b>100</b>	<b>500</b>	<b>25</b>

### Elective III:

#### Elective III Topics for 3 Credits

- 1 Value Education, Human Rights and Legislative Procedures
- 2 Environmental Studies
- 3 Renewable Energy Studies
- 4 Disaster Management
- 5 Foreign language
- 6 Knowledge Management
- 7 Economics for Engineers
- 8 Engineering Risk – Benefit Analysis

#### Elective III Topics for 2 Credits

- 1 Optimization Techniques
- 2 Fuzzy Mathematics
- 3 Design and Analysis of Algorithms
- 4 CUDA

## Second Year – Semester II

Sr.No.	Subject Code	Subject	Examination Scheme					Credits	
			Paper			Total			
			L/P	ISA	ESA		TW		OR
1	604206	Seminar III	5	--	----	50	50	100	5
2	604207	Project Stage II	20	--	---	150	50	200	20
		<b>Total</b>	<b>25</b>		<b>--</b>	<b>200</b>	<b>100</b>	<b>300</b>	<b>25</b>

**Note:** Seminar I, II & III reports should be prepared in Latex.



504201

## Digital CMOS Design

Credits: 04

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To learn MOSFET Models and layout fundamentals
2. To nurture students understanding in performance parameters of digital CMOS Design
3. To understand the advanced trends in CMOS design
4. To learn the delay models

### Course Outcomes:

On completion of the course, student will be able to -

1. Understand the fundamentals of CMOS Technology in Digital Domain
2. Explore the skills of designing digital VLSI
3. Demonstrate the ability of using EDA tools in IC Design

### Course Contents

#### Module I : MOSFET Models and Layout(10 Hrs)

MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE Models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams.

#### Module II : Performance parameters ( 10 Hrs)

Static, dynamic and short circuit power dissipations, Propagation delay, Power delay product, Fan in, fan out and dependencies. Delay Estimation: RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin.

#### Module III : Logic design ( 10 Hrs)

Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip-Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, case study; HDL codes for FSM, Meta-stability and solutions; Transmission gate, utility and limitations.

#### Module IV : Advanced trends (10 Hrs)

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Domino logic, NORA logic, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, High speed designs.

**References :**

1. Neil Weste and Kamaran, "Principles of CMOS VLSI Design", Education Asia.
2. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Pearson (Low Price Edition)
3. Charls Roth, "Digital System Design using VHDL", Tata McGraw Hill.
4. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill
5. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", PHI

**Laboratory Assignments/Experiments:**

1. To design, prepare layout and simulate CMOS Inverter for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc.
2. To design logic for ATM machine password and access functionality. Assume suitable I/Os such as card sense, 4 digit PIN number, type of account, amount, other facilities needed etc.
3. To design CMOS logic for  $F = A + B (C + D) + EFG$  and prepare layout. Assume suitable capacitive load & foundry. Measure  $T_R$ ,  $T_F$  &  $T_{PD}$ .
4. To draw FSM diagram, write HDL code, synthesis, simulate, place & route for Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. You may assume additional I/Os too.
5. To design and simulate combinational logic to demonstrate hazards. Also, simulate the same logic redesigned for removal of hazards.

504202

## Reconfigurable Computing

Credits: 04

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand various computing architectures
2. To provide students the concept of handling issues of reconfigure computing
3. To provide students implementation approaches of FPGA design in view of reconfiguration
4. To outline various applications reconfigure computing

### Course Outcomes:

On completion of the course, student will be able to –

- 1 Understand the concept of reconfigurable computing and its integration on computing platforms
- 2 Design, implement and analyze reconfigurable systems in the recent application domains using HDL
- 3 Use advanced EDA tools to simulate and synthesize HDL codes for reconfigurable architectures

### Course Contents

#### Module I : (10 Hrs)

Domain of RC: General Purpose Computing, Domain-Specific Processors, Application-Specific Processors, Reconfigurable Computing, Fields of Application. Architecture of Field Programmable Gate Arrays, Reconfigurable Processing Fabric (RPF) Architectures: Fine grained, Coarse-Grained, Integration of RPF into Traditional Computing Systems.

#### Module II : (10 Hrs)

Early systems of Reconfigurable computing: PAM, VCC, Splash, PRISM, Teramac, Cray, SRC, non-FPGA research, other issues; Reconfiguration Management: Reconfiguration, Configuration architectures, managing reconfiguration process, reducing reconfiguration time, configuration security.

#### Module III : (10 Hrs)

Implementation: Integration, FPGA Design Flow, System On A Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip. Reconfiguration Project Design Approaches: J-Bit, Modular, Early Access, Vivado.

#### Module IV : (10 Hrs)

RC Applications: Implementing applications with FPGAs, various applications and use of reconfiguration: Video Streaming, , Distributed arithmetic, Adaptive Controller, Adaptive cryptographic systems, Software Defined Radio, High-Performance Computing, Automatic target recognition systems.

### References :

- 1 Bobda Christophe, "Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications", Springer.
- 2 Hauck Scott, Dehon A, "Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation", Elsevier.
- 3 Vivado Partial Reconfiguration.pdf: user guide 909 by Xilinx Revision: 04/06/2016.

**Laboratory Assignments/Experiments:**

- 1 To design and implement a Multi Context (4) 4-LUT and implement using HDL and download on FPGA.
- 2 Top level modular and hierarchical designs of Adder and Subtractor such that they can be replaced.
- 3 An adaptive design of LED shifter (Right & Left shift)
- 4 SoPC based Hw-SW design (Soft/Hard Processor + FPGA HW)

504203

## Embedded System Design

**Credits: 4**

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand various design issues in embedded systems
2. To learn ARM 9 architecture and its programming concepts
3. To learn embedded LINUX operating system
4. To make aware of the significance of embedded network processors

### Course Outcomes:

On completion of the course, student will be able to –

1. Design ARM Processor based Embedded Systems
2. Carry out programming in Embedded programming in C, C++
3. Port Linux operating system and device drivers
4. Understand attributes of functional units of Network Protocol

### Course Contents

#### Module I :

( 10 Hrs)

Introduction to Embedded Systems: Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, Design Metrics, General Purpose Processor, System On chip. Embedded system design and development: Embedded system design, Life-Cycle Models, Development tools, Introduction to Development Platform Trends (only introduce IDE, board Details and Application) Arduino, Beaglebone, Raspberry PI, Intel Galileo Gen 2 .

#### Module II :

(10 Hrs)

ARM CORTEX series features, Improvement over classical series, CORTEX ARM processors series, Features and applications, Survey of CORTEX based controllers from various manufacturers, ARM-M3 Based Microcontroller LPC1768: Features, Architecture block diagram & its description, System Control, Clock & Power Control, Pin Connect Block. CMSIS Standard, Bus Protocols Ethernet, CAN, USB, Bluetooth.

#### Module III :

( 10 Hrs)

Embedded Linux: System architecture, BIOS versus boot-loader, Booting the kernel, Kernel initialization, Space initialization, Boot loaders and Storage considerations. Linux kernel construction: Kernel build system, Obtaining a custom Linux kernel, File systems, Device drivers, Kernel configuration.

#### Module IV : (10 Hrs)

Embedded System Design Case Studies: Design Case Studies like Automated Meter Reading Systems (AMR), Digital Camera, Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, Certification (EMI / RFI) and Documentation. Study of any two real life embedded products in detail.

## **References :**

1. [www.nxp.com/documents/user\\_manual/UM10360.pdf](http://www.nxp.com/documents/user_manual/UM10360.pdf).
2. Noergaard Tammy, "Embedded Systems Architecture", Elsevier Publication.
3. Hallinan Christopher, "Embedded Linux Primer: A Practical Real-World Approach", Second Edition, Pearson Education.
4. Shibu, "Introduction to Embedded Systems", TMH.
5. Comer D E, "Network System Design using Network Process", PHI.
6. Croeley Patrick, Franklin M. A , Hadimioglu H & Onufryk P Z, "Network Processor Design, Issues and Practices", vol-1-2, Elsevier.
7. Uyles Black, "Computer Networks-Protocols, Standards Interfaces", Second Edition , PHI.
8. <http://www.npforum.org/>; <http://www.intel.com/design/network/products/npfamily>.

## **Laboratory Assignments/Experiments:**

1. Write a program for 4\*4 Matrix Keypad Interface.
2. To develop character device driver for GPIO
3. One experiment based on any one of development Platform: Arduino, Beaglebon, Raspberry Pi, Intel Galileo Gen 2.
4. Interfacing USB & CAN of LPC 1768.
5. Write a program for External Interrupt.

504204

## Research Methodology

Credits: 4

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To learn the process of identification of research problem
2. To understand the importance of statistics involved in research
3. To understand the process of analysis and verification of developed system model
4. To develop a skill to prepare research proposals

### Course Outcomes:

On completion of the course, student will be able to-

1. Outline research problem, its scope, objectives and errors
2. Understand basic instrumentation schemes and its data collection methods
3. Learn various statistical techniques
4. Develop model and can predict the performance of experimental system
5. Write research proposals of their own domain

### Course Contents

#### Module I : ( 10 Hrs)

Research Problem: Meaning of research problem, Sources of research problem, Criteria/ Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Basic instrumentation: Instrumentation schemes, Static and dynamic characteristics of instruments used in experimental set up, Performance under flow or motion conditions, Data collection using a digital computer system, Linear scaling for receiver and fidelity of instrument, Role of DSP is collected data contains noise.

#### Module II : ( 10 Hrs)

Applied Statistics: Regression analysis, Parameter estimation, Multivariate statistics, Principal component analysis, Moments and response curve methods, State vector machines and uncertainty analysis.

#### Module III : (10Hrs)

Modelling and prediction of performance: Setting up a computing model to predict performance of experimental system, Multi-scale modelling and verifying performance of process system, Nonlinear analysis of system and asymptotic analysis, Verifying if assumptions hold true for a given apparatus setup, Plotting family of performance curves to study trends and tendencies, Sensitivity theory and applications.

#### Module IV : (10Hrs)

Developing a Research Proposal : Format of research proposal, Individual research proposal, Institutional proposal. Proposal of a student – a presentation and assessment by a review committee consisting of guide and external expert only. Other faculty members may attend and give suggestions relevant to topic of research.

**References :**

1. Melville Stuart, Goddard Wayne, "Research methodology: An Introduction for Science & Engineering students" .
2. Ranjit Kumar, "Research Methodology: A Step by Step Guide for Beginners", Second edition.
3. Dr. Kothari C R, "Research Methodology: Methods and Trends".
4. Dr. Sharma S D, KedarNath, "Operational Research".

**Laboratory Assignments/Experiments:**

1. Design a typical research problem using scientific method.
2. Design a data collection system using digital computer system.
3. Study the various analysis techniques.
4. Design and develop a computing model to predict the performance of experimental system.
5. Develop the following research proposal :A. Individual B. Institutional.





**References :**

1. Beeby S P, Ensell Graham, Michael Kraft and Neil White, “MEMS Mechanical Sensors” Artech House Publications, ISBN-10: 1580535364 /ISBN-13: 978-1580535366.
2. Kovacs, “Micro machined Transducers Sourcebook”, McGraw-Hill Publications, ISBN-10: 0072907223/ISBN-13:978-0072907223.
3. Gardner W, Varadan V K &Awadelkarim O O,“ Microsensors, MEMS and Smart Devices: Technology, Applications and Devices”, Julian Publications, ISBN-10: 047186109X/ISBN-13: 978-0471861096.
4. Kaajakari Ville,” Practical MEMS: Analysis and Design of Microsystems”, ISBN-10: 9780982299104, ISBN-13: 978-0982299104.
5. MalufNadim,WilliamsKirt, “ An Introduction to Microelectromechanical Systems Engineering”, John Willy & sons Ltd.ISBN-10: 1580535909/ ISBN-13: 978-1580535908.
6. Mohamed Gad-el-Hak,” The MEMS Handbook”, Second Edition , 3 Volume Set.
7. Stephen D. Senturia,” Microsystem Design”, Second edition.

**Laboratory Assignments/Experiments:**

- 1 To simulate the behavior of sensors and actuators for understanding micro motions.
- 2 To simulate gears to understand principle concepts of gear motion.
- 3 To explain Hooke’s law in understanding spring force using actuator and spring.
- 4 To explain ohm law by putting actuators in series and parallel.



**Laboratory Assignments/Experiments:**

- 1 Introduction of analysis and characterization of Nano structured materials, coating and thin film sensors.
- 2 Surface tension measurement of Nano fluids.
- 3 To observe size and slope of the Nano sized sample using scanning electron microscopy.
- 4 Design, simulation and analysis of Nano structures.



**References :**

- 1 NurmiJari, "Processor Design-System on Chip Computing for ASIC"s and FPGA", Springer Publications.
- 2 Frantz G, "The DSP and Its Impact on the Technology".
- 3 Leibson S, Tensilica, "Customizable Processors and Processor Customization".
- 4 Campi F, "Run-Time Reconfigurable Processors".
- 5 Garside J, Furber S, "Asynchronous and Self-Timed Processor Design".
- 6 Rusu S, "Processor Clock Generation and Distribution".
- 7 Dehon Andre, "Reconfigurable Architecture for General purpose Computing".

**Laboratory Assignments/Experiments:**

1. Design and implement MAC Unit on PLD
2. Design and implement CPU on PLD
3. Design and implement Carry look-ahead generator on PLD
4. Design and implementation of Translation look-aside buffer.



**Laboratory Assignments/Experiments:**

1. Reading data from Sensor node.
2. Implement 50 stationary nodes topology using NS2 for data transmission and record QoS parameters of the Networks/ Test bed.
3. Implement 50 dynamic nodes topology using NS2 for data transmission and record QoS parameters of the Networks /Test bed.
4. On any above topology change the Network layer/Transport layer/MAC layer protocol and monitor the changes between any two protocols/ test bed using Network Simulator.





**Laboratory Assignments/Experiments:**

1. Characterize n-MOSFET with the given model parameters, from the parameters students will reproduce I-V characteristics. Replace the model with any other SPICE model. Compare both the I-V characteristics.
2. Characterize p-MOSFET with the given model parameters, from the parameters students will reproduce I-V characteristics. Replace the model with any other SPICE model. Compare both the device I-V characteristics.
3. Characterize n-MOSFET and p-MOSFET to find out low frequency C-V characteristics behavior with the given model parameters.
4. Characterize n-MOSFET and p-MOSFET to find out high frequency C-V characteristics behavior with the given model parameters.
5. Characterize  $g_m/I_D$  of the MOS devices

**504206**

**Lab Practice I**  
**Credits: 4**

**Teaching Scheme:**

**Lectures : 4 Hrs/week**

**Examination Scheme:**

**TW : 50 Marks**

**OR : 50 Marks**

The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of that semester.

504207

## Analog CMOS Design

**Credits: 4**

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand theory of analog circuits using MOS small signal models
2. To understand design principles and techniques of CMOS Amplifiers
3. To gain design aspects of HF and Low Noise Amplifiers
4. To learn different methods of Stability and Frequency Compensation

### Course Outcomes:

On completion of the course, student will be able to-

1. Understand design concepts and issues of CMOS amplifiers
2. Learn different Compensation techniques
3. Acquire the knowledge of designing of HF and Low Noise Amplifiers

### Course Contents

#### Module I : (10Hrs)

Current sources and References : MOSFET as switch, diode and active resistor; MOS Small-signal Models, Common Source Amplifier, The CMOS Inverter as an Amplifier, Weak inversion; Short channel regime; Current sinks and sources; Current mirrors; Current and voltage references, band gap reference.

#### Module II : (10Hrs)

CMOS Amplifiers: Design of CMOS amplifiers, Inverting amplifiers, Cascode amplifiers, Differential amplifiers, Folded cascode; Current amplifiers, Output amplifier. Op Amps, high speed Op Amps, micro power Op Amps, low noise Op Amps.

#### Module III : (10 Hrs)

Comparators, Stability and Frequency Compensation: General considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps and Other compensation techniques.

#### Module IV : (10Hrs)

HF Amplifiers & Low Noise Amplifier: Open and Short circuit methods to estimate bandwidth, multistage amplifier for high bandwidth, Low Noise Amplifier (LNA) design, noise and power trade off, optimizations, Design of mixer, Advanced trends in Radio Frequency (RF) chip design.

#### References :

1. Thomas Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", Second edition, Cambridge.
2. Razavi B, "Design of Analog CMOS Integrated Circuits", McGraw-Hill.
3. Allen P E and Holberg D R, CMOS Analog Circuit Design, Second Edition, Oxford University Press.
4. Gray P, Hurst P. J, Lewis S. H and Meyer R, " Analysis and Design of Analog Integrated Circuits", Fourth edition, Wiley.

### **Laboratory Assignments/Experiments:**

1. To design cascode current mirror for output current of 100  $\mu\text{A}$ . Prepare layout and simulate. Comment on output resistance.
2. To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR.
3. To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technology for voltage gain of 60 dB, bandwidth of 100 MHz, and source impedance of 50  $\Omega$ .
4. To design CMOS RF amplifier for voltage gain of 60 dB. Suggest and design suitable technique to enhance the bandwidth. Simulate each added technique step by step. Comment on the improvement resulted each time. Prepare layout of the final schematic and simulate.
5. List the sources of cross talk. Explore in detail, the existence of cross talk in each case. Explain the mitigation techniques. Prepare case study for one of them. Verify the cross talk and its mitigation through simulation.

504208

## System on Chip

**Credits: 4**

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand the basic concepts and models inSoC
2. To exploreMicro-programmed Architectures and SoCmodeling
3. To explore features of simulation and synthesis of RTL intent
4. To learn recent trends in SoCdesign

### Course Outcomes:

On completion of the course, student will be able to –

1. Learn Design flow graphs and flow modeling
2. Understand SoC modeling and interfacing
3. Gain knowledge of SoC memory system design, embedded software and energy management techniques for SoC design, SoC prototyping, verification, testing and physical design
4. Design , implement and test SoC

### Course Contents

#### Module I : (10 Hrs)

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSM data-path, simulation and RTL synthesis, language mapping for FSM.

#### Module II : (10 Hrs)

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOCmodelling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces , coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model .

#### Module III : (10 Hrs)

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

#### Module IV : (10Hrs)

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS, SoC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

**References :**

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer Publications.
2. Sanjay Churiwala, SapanGarg , "Principles of VLSI RTL Design A Practical Guide", Springer Publications.
3. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on-Chip", Springer Publications.
4. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education.
4. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer Publications.

### Laboratory Assignments/Experiments:

1. Design, simulate and implement FSM on PLD for detection of either of input sequence  $X = \dots 1001\dots$  or  $\dots 1101\dots$  sequence and set output flags  $Y = "1"$  or  $Z = "1"$  respectively. What is effect on area, speed, fan out and power by implementing this design using different state encoding styles?
2. Design and implement MOD4 counter on PLD and verify multi-clock operations by probing logic analyzer

Control bits	Count update after every sec.
00	0.25 sec
01	0.5 sec
10	1 sec
11	4 sec

Why gated clock is not preferred in digital design? Write Verilog code to implement CMOS layout which will generate glitch also design a RTL by Write VHDL will generate glitch and also measure it using electronic test equipment.

3. Implement temperature logging system as a co-design by Interfacing FPGA &  $\mu$ C 8051 as follows :
  - i) LM 35 interfaced with ADC
  - ii) ADC interfaced with FPGA
  - iii) FPGA interfaced with  $\mu$ C 8051
  - iv)  $\mu$ C 8051 is interfaced with LCD
4. To display real-time room temperature. If temperature is greater than 250 C Bi-colors LED should change its normal

Green color to RED color via opto-isolator by actuation of relay



504209

## Embedded Automotive Systems

**Credits: 4**

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To introduce the potential of automotive systems in industries
2. To understand Automotive Sensory Systems
3. To explain the importance of Automotive control in system design
4. To make student aware of different Automotive protocols for internal communication

### Course Outcomes:

On completion of the course, student will be able to -

1. Understand the fundamentals of different Automotive Systems
2. Learn utility of sensors and instrumentation in vehicle systems
3. Design control system for various vehicular modules
4. Acquire knowledge of various automotive protocols
5. Provide technical embedded solutions for the development of automotive Systems

### Course Contents

#### Module I : (10 Hrs)

Automotive Systems Overview :Automotive Vehicle Technology, Overview of Vehicle Categories, Various Vehicle Sub Systems like Chassis, Body, Driveline, Engine technology, Fuelling technology, vehicle Emission, Brakes, Suspension, Emission, Doors, Dashboard instruments, Wiring Harness, Safety & Security , Comfort & Infotainment, Communication & Lighting, Future Trends in Automotive Embedded Systems : Hybrid Vehicles, Electric Vehicles.

#### Module II : (10Hrs)

Automotive Sensory System :Automotive Sensors and Transducers: Temperature, Manifold and Barometric Pressures, Humidity, Carbon Dioxide (CO<sub>2</sub>), Carbon Monoxide (CO), Oxygen (O<sub>2</sub>) Sensor, Proximity Distance Sensors, Engine Speed sensor, Throttle Position Sensor, Pressure Sensors, Knock Sensor & Mass Flow Sensor. Typical Sensors Specifications & Microcontroller Interface Considerations, Sensor Calibration, Curve fitting.

#### Module III : (10Hrs)

Automotive Control System Design:Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Anti-locking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering.

#### Module IV : (10 Hrs)

Automotive Protocols :The need for Protocol , Automotive Protocols : LIN, CAN, KWP2000 & J1939, FlexRay, Test, Calibration and Diagnostics tools for networking of electronic systems like ECU Software and Testing Tools , ECU Calibration Tools , Vehicle Network Simulation. Advanced Trends in Automotive Electronics: AUTOSAR Architecture.

**References :**

1. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Perspective", Seventh edition, Butterworth-Heinemann Publications.
2. Ronald K. Jorgen, "Automotive Electronics Handbook", Mc-Graw Hill.
3. Kiencke, Uwe, Nielsen&Lars, "Automotive Control Systems for Engine, Driveline and Vehicle", Second edition, Springer Publication.
4. Tao Zhang, Luca Delgrossi, "Vehicle Safety Communications: Protocols, Security and Privacy", Wiley Publication.
5. Robert Bosch," Automotive Hand Book", Fifth edition, SAE Publications.

**Laboratory Assignments/Experiments:**

1. Write a program for Sensing Engine Speed, Load and Temperature.
2. Develop a transistorized Ignition Driver.
3. Design a single cylinder engine Management System.
4. Perform a case study for any two automotive protocols.
5. Study the functional design aspects of Hybrid Automotive Systems.

504210

## Embedded Product Design (Elective II)

**Credits: 5**

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand design challenges of embedded hardware and software
2. To gain knowledge of testing and verification issues in design cycle
3. To introduce h/w and s/w design models with different technology
4. To learn the importance of documentation for technology transfer

### Course Outcomes:

On completion of the course, student will be able to-

1. Learn specifications and design challenges of embedded products
2. Estimate cost of embedded product
3. Understand the aspects of Mechanical Packaging, Testing, reliability and failure analysis, EMI/RFI Certification and Documentation
4. Demonstrate the knowledge of embedded product design related hardware and software design tools

### Course Contents

#### Module I : (10Hrs)

Overview of Embedded Products: Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components, Iteration and refinement of the partitioning.

#### Module II : (10Hrs)

Design Models and Techniques: various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology.

#### Module III : (10Hrs)

Modules of Hardware and Software: Tradeoffs, Custom Single-purpose processors, General-purpose processors, Software, Memory, Interfacing, Design technology-Hardware design, FPGA design, firmware design, driver development, RTOS porting, cost reduction, re-engineering, optimization, maintenance, validation and development, prototyping, turnkey product design.

#### Module IV : (10Hrs)

Testing and verification: Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion. Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, communication protocols, Certification (EMI/ RFI) and its documentation. Study of any two real life embedded products in detail.

#### References :

1. Vahid Frank and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley Publication.
2. Marwedel P, "Embedded System Design", Springer Publication.

**Laboratory Assignments/Experiments:**

1. To estimate techno-commercial feasibility of any one embedded product such as mobile phone, programmable calculator, tablet PC, biometrics system, set top box etc.
2. To study design considerations of any one embedded product e.g. laptop, video conferencing system, surveillance/ security system, EMG/ECG machine etc.
3. To design any one embedded product to solve any real life problems.
4. To test the hardware designed for above assignment (3) using suitable simulation tool.
5. To simulate the software designed for the above assignment (3) using suitable simulation tool.

504210

## High Speed ICs (Elective II)

Credits: 5

### Teaching Scheme:

Lecture :4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand basic design aspects of high frequency circuits
2. To explain different characteristics of high speed logic families
3. To learn design issues of interconnects in High Speed Circuit Design

### Course Outcomes:

On completion of the course, student will be able to –

1. Acquire knowledge about High Speed VLSI Circuits Design
2. Identify the basic need of high speed digital logic families
3. Understand various types VLSI interconnections
4. Analyze various interconnection delay models
5. Acquire insights of nanotechnology circuits interconnections

### Course Contents

#### Module I : (10Hrs)

A brief history of high-frequency integrated circuits and its design, High-frequency circuits in wireless, fiber-optic and imaging systems.

#### Module II : (10 Hrs)

High-speed digital logic families, Design methodology for maximum data rate, Bi-CMOS MOS-HBT logic, Pseudo-CML logic, Other bipolar, MOS and Bi-CMOS CML, and ECL gates, CML/ECL gate layout techniques.

#### Module III : (10Hrs)

Metal-Insulator-Semiconductor Microstrip Line Model of an Interconnection., Transmission Line Analysis of Single Level Interconnections, Transmission Line Analysis of Parallel Multilevel Interconnections, Very High Frequency Losses in a Microstrip Interconnection, Compact Expressions for Interconnection Delays, Interconnection Delays in Multilayer Integrated Circuits

#### Module IV : (10Hrs)

High Speed Circuit Design: High Speed Properties of logic gates-power, speed and packaging. Cross talk in solid ground and slotted ground planes, Near end and Far end cross talk. End terminators and cross talk in terminators, Vias and its characteristics. Stable voltage references, Connectors and cross talk due to connectors. Clock jitter and signal integrity mechanism for high speed link. Clock and power distribution related problems.

#### References :

1. Voinigescu Sorin, "High-Frequency Integrated Circuits", Cambridge University Press.
2. Goel A K, "High-Speed VLSI Interconnections", Second edition, Wiley-IEEE Press.
3. Nakhla M S, Zhang O J, "Modeling and Simulation of High Speed VLSI Interconnects", Springer Publication.
4. Ludwig Reinhold, Bretchko Pavel, "RF Circuit Design Theory and Applications", Pearson education.
5. Howard Johnson, Graham Martin, "High Speed digital Design-A Handbook of Black Magic", Pearson education.

**Laboratory Assignments:**

1. Simulate RC circuit and comment on transient response.
2. Simulate startup model of RLC.
3. Simulate a transmission line to evaluate VSWR, reflection coefficient parameters considering different loading considerations using analog simulation tool.
4. Plot stability circle, for given values of S parameters.

504210

## Mixed Signal IC Design(Elective II)

**Credits: 5**

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To introduced Mixed Signal layout issues in circuit design
2. To explain the Architectures of ADC and DAC
3. To acquire knowledge on Modeling Data Convertors

### Course Outcomes:

On completion of the course, student will be able to-

1. Understand the mixed signal issues in circuit design
2. Learn modeling different ADC and DAC
3. Apply methods to improve SNR
4. Explore the operation of delta-sigma/ sigma-delta converterand their issues

### Course Contents

#### Module I : (10 Hrs)

Analog versus discrete time signals, Converting analog signal to digital signal, Sample and hold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floor planning, power supply and grounding issues, fully differential design/ matching, guard rings, shielding, interconnect considerations.

#### Module II : (10Hrs)

DAC architectures: Resistor string, R-2R ladder networks, Current steering, Charge-scaling, Pipeline. ADC architectures: Flash, Pipeline, Dual slope, Successive approximation, Oversampling ADC.

#### Module III : (10Hrs)

Data converter modeling: Sampling and aliasing: A modeling approach, Impulse sampling, AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectral response, Circuit concerns for implementing S/H. Quantization noise, RMS quantization noise voltage, treating quantization noise as a random variable, calculating RMS quantization noise voltage from a spectrum

#### Module IV : (10Hrs)

Data converter SNR: Effective number of bits, Signal to noise plus distortion ratio, Spurious free dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR, Spectral density view, Jitter and averaging, Relaxed requirements on AAF, Data converter linearity requirements, Adding noise dither to ADC input, Decimating filters for ADC. Decimating filters for ADCs, Interpolating filters for DACs. Noise-shaping data converters: First order noise shaping, Second order noise shaping, Noise shaping topologies: Higher-order modulators, Miltibit modulators, Cascaded modulators.

**References :**

1. Baker R J, "CMOS: Mixed Signal Circuit Design", Second edition, Wiley IEEE Press Publications.
2. Baker R J, "CMOS: Circuit Design, Layout and Simulation", Second edition, Wiley IEEE Press Publications.
3. Allen, Phillip E., Holberg, Douglas R., "CMOS Analog Circuit Design", Oxford University Press Publications.

**Laboratory Assignments/Experiments:**

1. Plot ideal transfer curves for 3 bit and 4 bit DAC, using  $V_{\text{Ref}} = 5\text{V}$  and  $3\text{V}$ . Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments.
2. For 3 bit ADC,  $V_{\text{Ref}} = 5\text{V}$ , Plot ideal transfer curve and quantization error.
3. Plot transfer curve and quantization error by shifting entire transfer curve of example 2, left by 1/2 LSB and calculate DNL.
4. Design and simulate anti-aliasing filter with two input sine waves having frequencies 4 MHz and 40 MHz.
5. Design and simulate sample and hold circuit, with 8 MHz sine wave sampled at 100 MHz.
6. Calculate SNR and plot ADC input and DAC output for cascaded 8 bit ADC and DAC operated on  $V_{\text{DD}}=1.5\text{ V}$ ,  $V_{\text{in}} = 24\text{ mV}$  (0.75VPP) and Sampling frequency = 100 MHz.



## 504210 Embedded Signal Processor Architectures (Elective II)

**Credits: 5**

### Teaching Scheme:

Lecture : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To impart knowledge on the theoretical aspects of signal analysis and processing
2. To explore DSP Processor architectures
3. To understand DSP algorithms
4. To elaborate real world DSP applications

### Course Outcomes:

On completion of the course, student will be able to-

1. Designing system with linear filters using DFT
2. Develop technical abilities of designing any applications with FIR and IIR filters
3. Port algorithms on DSP Processor Platforms
4. Design Adaptive filters
5. Analyze filter structures

### Course Contents

#### Module I : (10Hrs)

Signal Analysis and Processing: Discrete Fourier Transform, Fast Fourier Transform, Design of FIR Filters using windowing technique, Design of IIR Filters through Impulse invariance and bilinear transformation technique, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters.

#### Module II : (10 Hrs)

Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, Real time implementation Considerations, Memory System and Data Transfer, Code Optimization.

#### Module III : (10Hrs)

Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph. Iteration bounds: Critical Path, Loop Bound, Algorithm to compute iteration bound, Longest Path Matrix (LPM).

#### Module IV : (10Hrs)

Practical DSP Applications: Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.

## References :

1. Woon-Seng Gan, Sen M. Kuo, "Embedded Signal Processing With the Micro Signal Architecture", Wiley-IEEE Press.
2. Kuo Sen M, Woon-Seng Gan, "Digital Signal Processors: Architectures, Implementations and Applications", Prentice-Hall.
3. Proakis J G, Manolakis D G, "Digital Signal Processing ,Principles, Algorithms and Applications", Prentice-Hall.
4. Lawrence R. R, Bernard Gold, "Theory and Application of Digital signal Processing", Prentice-Hall.
5. Parhi Keshab , "VLSI Digital Signal Processing System", Wiley Publication.

## Laboratory Assignments/Experiments:

1. Design and simulate N point FFT by targeting DSP processor platform.
2. Design and simulate N tap FIR filter by targeting suitable DSP processor platform.
3. Design and simulate LMS adaptive filter.
4. Design a system for DTMF signal detection. Write a program to detect the DTMF signal using Goertzel algorithm
5. Performance comparison of different filter structure.
6. Record a speech file in your own voice with sampling frequency of 8000 Hz. Design a system to decompose a speech signal using Daubechies wavelet using wavelet packet decomposition. Write a program to implement the system and plot the speech signal passed via each wavelet filter.

504210

## Real Time Operating Systems (Elective II)

Credits: 05

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To understand software Architecture and Development cycle of Operating Systems
2. To learn various management attributes of Operating System
3. To understand RTOS
4. To study Linux/ RT Linux environment

### Course Outcomes:

On completion of the course, student will be able to-

1. List Embedded Software Developments Tools
2. Learn Software Development Process Life Cycle
3. Gain knowledge of Real Time Operating Systems with respect to uCOS
4. Understand RT Linux operating System

### Course Contents

#### Module I : (10 Hrs)

Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance

#### Module II : (10Hrs)

Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model

#### Module III : (10Hrs)

Real Time Operating Systems ( $\mu$ C/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting  $\mu$ Cos-II.

#### Module IV : (10Hrs)

Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.

### References :

1. Labrossy J. J, Lawrence, “ $\mu$ C/OS-II, The real time Kernel”, R & D Publication.
2. Dr Prasad K V K K, “Embedded Real Time Systems: Concepts, Design & Programming”, Dreamtech Publication.
3. Simon D. E, “An Embedded Software Primer”, Pearson education.
4. Tanenbaum A S, “Modern Operating Systems”, Prentice Hall.
5. Raj Kamal, “Embedded Systems Architecture, Programming and design”, Tata Mc-Graw-Hill.

**Laboratory Assignments/Experiments:**

1. Multitasking in  $\mu$ COS- II RTOS using minimum 3 tasks on ARM7. ( $\mu$ COS - II based Experiments).
2. Semaphore as signaling and synchronizing on ARM7. ( $\mu$ COS - II based Experiments).
3. Write a program for 4\*4 Matrix Keypad Interface ( based on Linux Operating System).
4. Develop character device driver for GPIO (based on Linux Operating System).
5. Write a program for External Interrupt (based on Linux Operating System).

504211

**Lab Practice II**  
**Credits: 4**

**Teaching Scheme:**

**Lectures : 4 Hrs/week**

**Examination Scheme:**

**Term Work : 50 Marks**  
**Oral : 50 Marks**

The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of the semester.

504212

**Seminar I**

**Credits: 4**

**Teaching Scheme:**

**Lectures : 4 Hrs/week**

**Examination Scheme:**

**Term Work : 50 Marks**

**Oral : 50 Marks**

**Seminar I:** Shall be on state of the art topic of student's own choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

604201

## Testing and Verification of VLSI Circuits

**Credits: 4**

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To introduce design process in VLSI
2. To understand the logical and Fault simulation models
3. To learn techniques for design of testability
4. To study hardware and software verification issues for testing

### Course Outcomes:

On completion of the course, student will be able to-

1. Accept challenges in VLSI Testing at different abstraction levels
2. Understand fault models for generation of test vectors
3. Calculate observability and controllability parameters of circuit
4. Enhance testability of a circuit
5. Use simulation techniques for designing and testing of VLSI circuits
6. Identify characteristics of verification methods

### Course Contents

#### Module I : (10Hrs)

Introduction to the concepts and techniques of VLSI (Very Large Scale Integration) design verification and testing, VLSI testing process and test equipment, test economics and product quality, fault modeling, testing and verification in VLSI design process.

#### Module II : (10 Hrs)

Test methods, logic and fault simulation, modeling circuits for simulation, algorithms for true-value simulation, algorithms for fault simulation, statistical methods for fault simulation, testability measures, combinational circuit test generation, sequential circuit test generation, memory test.

#### Module III : (10Hrs)

Design for testability, Scan and Boundary scan architectures, Built-in Self-test (BIST) and current-based testing, analog test bus standard.

#### Module IV : (10Hrs)

System test and core-based design, ATPG, Embedded core test fundamentals. Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

**References :**

- 1 Bushnell M L, Agrawal V D, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers.
- 2 Abramovici M, Breuer M A and Friedman A D, “Digital systems and Testable Design”, Jaico Publications.
- 3 Crouch A L, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall.
- 4 Kropf T, “Introduction to Formal Hardware Verification,” Springer Publications.

**Laboratory Assignments / Experiments:**

1. Write VHDL/Verilog code for MUX -D scan cell and Level Sensitive/edge triggered MUX - D scan cell.
2. Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
3. To develop an exhaustive test bench for lower level combinational designs: a. Adder and b. Multiplexer.
4. To prepare a complete Test vector set for all possible stuck at faults parity checker where the data word is of 2-bit.



604202

## ASIC Design

**Credits: 4**

### Teaching Scheme:

Lectures : 4 Hrs/week

### Examination Scheme:

In-Sem : 50 Marks  
End-Sem : 50 Marks

### Course Objectives:

1. To gain knowledge of the process of designing application specific algorithm for ASIC
2. To synthesize designs in EDA tool environment
3. To learn design methodologies, simulation and verification
4. To learn issues in Mixed signal ASIC design

### Course Outcomes:

On completion of the course, student will be able to-

1. Understand concepts and techniques of ASIC modeling and synthesis
2. Perform static timing analysis, delay estimation and synchronization
3. Learn ASIC Construction and testing techniques

### Course Contents

#### Module I : (10 Hrs)

ASIC Modeling and Synthesis :IC Design Technologies, Types of ASIC and Comparisons, ASIC Design Flow, Logic Synthesis, Simulation, EDA Tools, HDL Based logic Design and Test bench, library, logic level optimization.

#### Module II : (10Hrs)

ASIC Physical Design :System Specifications, Architecture Design, Logic and Circuit Design, Physical Design, CAD Tools, System partitioning, Estimating ASIC Size, Power Dissipation, Partitioning Strategies, Floor planning, Placement, Routing, Design Reuse.

#### Module III : (10 Hrs)

ASIC Timing Analysis: Static timing analysis, Timing constraints, false path detection, Timing optimization, ASIC library design, Delay estimation, mixed mode design and simulation, SI issues.

#### Module IV : (10 Hrs)

ASIC Verification and Testing:Different Chip Test Methods, Fault Models, Scan Test, Partial Test, Digital scan standards, BIST architecture, Memory Testing, BILBO, Boundary Scan, Self Test, JTAG, ATPG. Mixed Signal ASIC Design: Mixed Signal ASIC Design, Practical aspects of mix analog digital design, Gate level mixed mode simulation. A brief introduction to signal integrity effects in ASIC design, Synthesis and Testing.

### References :

- 1 Smith Michael, "Application Specific Integrated Circuits" Pearson Education.
- 2 Soin R S, Maloberti F, Franca J, "Analogue-digital ASICs: circuit techniques, design tools and applications", IEE Publications.
- 3 Singh Raminderpal, "Signal Integrity Effects in Custom IC and ASIC Designs", Wiley Publications.

**Laboratory Assignments / Experiments:**

1. Write HDL code to simulate, synthesis, and place & route memory on PLD. Check results and also write the test bench.
2. Write HDL code to simulate, synthesis, place & route FIFO on PLD. Check results and also write the test bench.
3. Draw CMOS layout & simulate shift register by applying DRC's of appropriate foundry using backend tool and check the output.
4. Draw CMOS layout & simulate 16:1 MUX by applying DRC's of appropriate foundry using backend tool and check the output.
5. Simulate Stuck at fault model of given function.

### Elective-III

Select one subjects from Group-I, and one subject from Group-II from the following list as Elective-III.

Group		Subject	Credit
I	1	Value Education, Human Rights and Legislative Procedures	3
	2	Environmental Studies	3
	3	Renewable Energy Studies	3
	4	Disaster Management	3
	5	Knowledge Management	3
	6	Foreign Language	3
	7	Economics for Engineers	3
	8	Engineering Risk – Benefit Analysis	3
II	1	Optimization Techniques	2
	2	Fuzzy Mathematics	2
	3	Design and Analysis of Algorithms	2
	4	CUDA	2

**604203A Value Education, Human rights and Legislative procedures (Elective III)  
Credits:3**

**Teaching Scheme:**

**Lectures: 3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Values and Self Development-Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non moral valuation, Standards and principles, Value judgments. Importance of cultivation of values, Sense of duty, Devotion, Self reliance, Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity, Power of faith, National unity, Patriotism, Love for nature, Discipline.

**Module II :**

**( 8 Hrs )**

Personality and Behavior Development- Soul and scientific attitude, God and scientific attitude, Positive thinking, Integrity and discipline, Punctuality, Love and kindness, Avoiding fault finding, Free from anger, Dignity of labor, Universal brotherhood and religious tolerance, True friendship, Happiness vs. suffering love for truth, Aware of self destructive habits, Association and cooperation, Doing best, Saving nature.

**Module III :**

**( 8 Hrs )**

Human Rights- Jurisprudence of human rights nature and definition, Universal protection of human rights, Regional protection of human rights, National level protection of human rights, Human rights and vulnerable groups. Legislative Procedures- Indian constitution, Philosophy, fundamental rights and duties, Legislature, Executive and Judiciary, Constitution and function of parliament, Composition of council of states and house of people, Speaker, Passing of bills, Vigilance, Lokpal and functionaries References

**References**

1. Chakraborty, S.K., Values and Ethics for Organizations Theory and Practice, Oxford University Press, New Delhi, 2001.
2. Kapoor, S.K., Human rights under International Law and Indian Law, Prentice Hall of India, New Delhi, 2002.
3. Basu, D.D., Indian Constitution, Oxford University Press, New Delhi, 2002.
4. Frankena, W.K., Ethics, Prentice Hall of India, New Delhi, 1990.
5. Meron Theodor, Human Rights and International Law Legal Policy Issues, Vol. 1 and 2, Oxford University Press, New Delhi, 2000.

**604203A**

**Environmental studies (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures: 3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Introduction and Natural Resources: Multidisciplinary nature and public awareness, Renewable and nonrenewal resources and associated problems, Forest resources, Water resources, Mineral resources, Food resources, Energy resources, Land resources, Conservation of natural resources and human role. Ecosystems: Concept, Structure and function, Producers composers and decomposers, Energy flow, Ecological succession, Food chains webs and ecological pyramids, Characteristics structures and functions of ecosystems such as Forest, Grassland, Desert, Aquatic ecosystems.

**Module II :**

**( 8 Hrs )**

Environmental Pollution- Definition, Causes, effects and control of air pollution, water pollution, soil pollution, marine pollution, noise pollution, thermal pollution, nuclear hazards, human role in prevention of pollution, Solid waste management, Disaster management, floods, earthquake, cyclone and landslides.

**Module III :**

**( 8 Hrs )**

Social issues and Environment- Unsustainable to sustainable development, Urban problems related to energy, Water conservation and watershed management, Resettlement and rehabilitation, Ethics, Climate change, Global warming, Acid rain, Ozone layer depletion, Nuclear accidents, holocaust, Waste land reclamation, Consumerism and waste products, Environment protection act, Wildlife protection act, Forest conservation act, Environmental issues in legislation, population explosion and family welfare program, Environment and human health, HIV, Women and child welfare, Role of information technology in environment and human health.

**References**

1. Agarwal, K.C., "Environmental Biology", Nidi Publication Ltd., Bikaner, 2001.
2. BharuchaErach, "Biodiversity of India," Mapin Publishing Pvt. Ltd., Ahmadabad, 2002.
3. Bukhootsow, B., "Energy Policy and Planning", Prentice Hall of India, New Delhi, 2003.
4. Cunningham, W.P., " Environmental Encyclopedia", Jaico Publishing House, Mumbai, 2003.

**604203A**

**Renewable Energy Studies (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures:3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I : Solar Energy:**

**( 8 Hrs )**

Photovoltaic Systems: Introduction to the Major Photovoltaic System Types, Current–Voltage Curves for Loads, Grid-Connected Systems: Interfacing with the Utility, DC and AC Rated Power, The “Peak-Hours” Approach to Estimating PV Performance, Capacity Factors for PV Grid Connected Systems, PV Powered Water Pumping, PV systems – off grid systems and scope for inclusive growth of rural India.

**Module II :Wind Energy:**

**( 8 Hrs )**

Wind Energy: wind speed and power relation, power extracted from wind, wind distribution and wind speed predictions. Wind power systems: system components, Types of Turbine, Choice of generators, electrical load matching, power control, Effect of wind speed variations, tower height and its effect, Variable speed operation, maximum power operation, control systems, Design consideration of wind farms and control

**Module III : Other Energy Sources:**

**( 8 Hrs )**

Biomass – various resources, energy contents, technological advancements, conversion of biomass in other form of energy – solid, liquid and gases. Gasifiers, Biomass fired boilers, Co-firing, Generation from municipal solid waste, Issues in harnessing these sources. Mini and micro hydel plants scheme layout economics. Tidal and wave energy, Geothermal and Ocean-thermal energy conversion (OTEC) systems – schemes, feasibility and viability. Fuel cell- types and operating characteristics, efficiency, energy output of fuel cell

**References**

1. Renewable energy technologies - R. Ramesh, Narosa Publication.
2. Energy Technology – S. Rao, Parulkar
3. Non-conventional Energy Systems – Mittal, Wheelers Publication.
4. Clark W. Gellings, “The Smart Grid: Enabling Energy Efficiency and Demand Response”,CRC Press
5. Renewable Energy Technologies – Chetan Singh Solanki, PHI Learning Pvt. Ltd.

**604203A**

**Disaster Management (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures: 3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Introduction :Concepts and definitions: disaster, hazard, vulnerability, risk, capacity, impact, prevention, mitigation). Disasters classification; natural disasters (floods, draught, cyclones, volcanoes, earthquakes, tsunami, landslides, coastal erosion, soil erosion, forest fires etc.); manmade disasters (industrial pollution, artificial flooding in urban areas, nuclear radiation, chemical spills etc); hazard and vulnerability profile of India, mountain and coastal areas, ecological fragility

**Module II :**

**( 8 Hrs )**

Disaster Impacts :Disaster impacts (environmental, physical, social, ecological, economical, political, etc.); health, psycho-social issues; demographic aspects (gender, age, special needs); hazard locations; global and national disaster trends; climate-change and urban disasters.

**Module III :**

**( 8 Hrs )**

Disaster Risk Reduction (DRR) : Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; structural and non-structural measures; risk analysis, vulnerability and capacity assessment; early warning systems, Post-disaster environmental response (water, sanitation, food safety, waste management, disease control); Roles and responsibilities of government, community, local institutions, NGOs and other stakeholders; Policies and legislation for disaster risk reduction, DRR programmes in India and the activities of National Disaster Management Authority.

**References**

1. <http://ndma.gov.in/> (Home page of National Disaster Management Authority).
2. <http://www.ndmindia.nic.in/> (National Disaster management in India, Ministry of Home Affairs).
3. PradeepSahni, 2004, Disaster Risk Reduction in South Asia, Prentice Hall.
4. Singh B.K., 2008, Handbook of Disaster Management: techniques & Guidelines, Rajat Publication.
5. Ghosh G.K., 2006, Disaster Management,APH Publishing Corporation.

**604203A**

**Knowledge Management (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures:3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Introduction: Definition, evolution, need, drivers, scope, approaches in Organizations, strategies in organizations, components and functions, understanding knowledge; Learning organization: five components of learning organization, knowledge sources, and documentation. Essentials of Knowledge Management; knowledge creation process, knowledge management techniques, systems and tools.

**Module II :**

**( 8 Hrs )**

Organizational knowledge management; architecture and implementation strategies, building the knowledge corporation and implementing knowledge management in organization. Knowledge management system life cycle, managing knowledge workers, knowledge audit, and knowledge management practices in organizations, few case studies

**Module III :**

**( 4 Hrs )**

Futuristic KM: Knowledge Engineering, Theory of Computation, Data Structure.

**References**

1. Knowledge Management – a resource book – A Thothathri Raman, Excel, 2004.
2. Knowledge Management- Elias M. AwadHasan M. Ghazri, Pearson Education
3. The KM Toolkit – Orchestrating IT, Strategy & Knowledge Platforms, AmritTiwana, Pearson, PHI, II Edn.
4. The Fifth Discipline Field Book – Strategies & Tools For Building A learning organizationPeterSenge et al. Nicholas Brealey 1994
5. Knowledge Management – Sudhir Warier, Vikas publications
6. Leading with Knowledge, MadanmohanRao, TataMc-Graw Hill.



**604203A**

**Foreign Language (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures:3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Pronunciation guidelines; Single vowels, Accentuated vowels, Vowels and consonants combinations, Consonants; Numbers 1-10 Articles and Genders; Gender in French, Plural articles, Some usual expressions. Pronouns and Verbs; The verb groups, The pronouns, Present tense, Some color Adjectives and Plural ; Adjectives, Some adjectives, Our first sentences, More Numbers.

**Module II :**

**( 8 Hrs )**

Sentences Structures; Some Prepositions, Normal Sentences, Negative Sentences, Interrogative Sentences, Exercises The Family; Vocabulary ,Conversation, Notes on Pronunciation, Notes on Vocabulary, Grammar, Liaisons Guideline. D'oùviens-tu (Where do you come from); Vocabulary, Conversation, Notes on Vocabulary, Liaisons Guidelines . Comparer (Comparing); Vocabulary, Conversation, Notes on Vocabulary, Grammar Liaisons Guidelines, Ordinal Numbers

**Module III :**

**( 8 Hrs )**

Le temps (Time); Vocabulary, Grammar, Time on the clock Additional French Vocabulary; Vocabulary related to - The Family, Vocabulary related to - Where do you come from? French Expressions and Idioms; Day-to-day Life, At Work, The car, Sports, Special Events Other French Flavours; Nos cousins d'Amérique - Québec et Accadie, Au pays de la bière et des frites, Mettez-vous à l'heure Suisse, VÉ, peuchère, le françaisbien de chez nous

**References**

<http://www.jump-gate.com/languages/french/index.html>

**604203A**

**Economics for Engineers (Elective III)**

**Credits:3**

**Teaching Scheme:**

**Lectures: 3 Hrs/Week**

**Examination Scheme:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 8 Hrs )**

Introduction to the subject: Micro and Macro Economics, Relationship between Science, Engineering, Technology and Economic Development. Production Possibility Curve, Nature of Economic Law, Time Value of Money: concepts and application. Capital budgeting; Traditional and modern methods, Payback period method, IRR, ARR, NPV, PI (with the help of case studies)

**Module II :**

**( 8 Hrs )**

Meaning of Production and factors of production, Law of variable proportions and returns to scale. Internal and external economies and diseconomies of scale. Concepts of cost of production, different types of costs; accounting cost, sunk cost, marginal cost, Opportunity cost. Break even analysis, Make or Buy decision (case study). Relevance of Depreciation towards industry. Meaning of market, types of market, perfect competition, Monopoly, Monopolistic, Oligopoly. (Main features). Supply and law of supply, Role of demand and supply in price determination.

**Module III :**

**( 8 Hrs )**

Indian Economy, nature and characteristics. Basic concepts; fiscal and monetary policy, LPG, Inflation, Sensex, GATT, WTO and IMF. Difference between Central bank and Commercial banks

**References :**

1. Jain T.R., Economics for Engineers, VK Publication
2. Singh Seema, Economics for Engineers, IK International
3. Chopra P. N., Principle of Economics, Kalyani Publishers
4. Dewett K. K., Modern economic theory, S. Chand
5. H. L. Ahuja., Modern economic theory, S. Chand

**604203A                      Engineering risk – Benefit and Analysis (Elective III)**  
**Credits:3**

**Teaching Scheme:**

**Lectures: 3 Hrs/Week**

**Examination Scheme\*:**

**In-Sem                      : 50 Marks**

**End-Sem                    : 50 Marks**

**Module I :** **( 8 Hrs )**

Introduction- Knowledge and Ignorance, Information Uncertainty in Engineering Systems, Introduction and overview of class; definition of Engineering risk; overview of Engineering risk analysis. Risk Methods: Risk Terminology, Risk Assessment, Risk Management and Control, Risk Acceptance, Risk Communication, Identifying and structuring the Engineering risk problem; developing a deterministic or parametric model System Definition and Structure: System Definition Models, Hierarchical Definitions of Systems, and System Complexity.

**Module II :** **( 8 Hrs )**

Reliability Assessment: Analytical Reliability Assessment, Empirical Reliability Analysis Using Life Data, Reliability Analysis of Systems

**Module III :** **( 8 Hrs )**

Reliability and probabilistic risk assessment (RPRA), decision analysis (DA), and cost-benefit analysis (CBA). All of these pertain to decision making in the presence of significant uncertainty. In ERBA, the issues of interest are: The risks associated with large engineering projects such as nuclear power reactors, the International Space Station, and critical infrastructures; the development of new products; the design of processes and operations with environmental externalities; and infrastructure renewal projects.

**References**

1. Risk Analysis in Engineering and Economics, B. M. Ayyub, Chapman-Hall/CRC Press, 2003.
2. Hoyland, Arnljot, and Rausand, Marvin. System Reliability Theory. Hoboken, NJ: WileyInterscience, 1994. ISBN: 9780471471332.
3. Clemen, Robert, — Making Hard Decisions: An Introduction to Decision Analysis (Business Statistics) — PHI publications

**604203B**

**Optimization Techniques (Elective III)**

**Credits:2**

**Teaching Scheme:**

**Lectures: 2 Hrs/Week**

**Examination Scheme\*:**

**In-Sem : 50 Marks**

**End-Sem : 50 Marks**

**Module I :**

**( 6 Hrs )**

First and second order conditions for local interior optima (concavity and uniqueness), Sufficient conditions for unique global optima; Constrained optimization with Lagrange multipliers; Sufficient conditions for optima with equality and inequality constraints;

**Module II :**

**( 8 Hrs )**

Recognizing and solving convex optimization problems. Convex sets, functions, and optimization problems. Least-squares, linear, and quadratic optimization. Geometric and semidefinite programming. Vector optimization. Duality theory. Convex relaxations. Approximation, fitting, and statistical estimation. Geometric problems. Control and trajectory planning

**Books:**

1. Stephen Boyd and LievenVandenberghe, Convex Optimization, Cambridge University Press.
2. A. Ben-Tal, A. Nemirovski, Lectures on Modern Convex Optimization: Analysis, Algorithms, and Engineering Applications, SIAM.
3. D. P. Bertsekas, A. Nedic, A. E. Ozdaglar, Convex Analysis and Optimization, Athena Scientific.
4. D. P. Bertsekas, Nonlinear Programming, Athena Scientific.
5. Y. Nesterov, Introductory Lectures on Convex Optimization: A Basic Course, Springer.
6. J. Borwein and A. S. Lewis, Convex Analysis and Nonlinear Optimization: Theory and Examples, Springer.

**604203B                      Fuzzy Mathematics (Elective III)**  
**Credits:2**

**Teaching Scheme:**

**Lectures: 2 Hrs/Week**

**Examination Scheme\*:**

**In-Sem                      : 50 Marks**

**End-Sem                    : 50 Marks**

**Module I :** **( 8 Hrs )**

Definition of a Fuzzy set; Elements of Fuzzy logic. Relations including, Operations, reflexivity, symmetry and transitivity; Pattern Classification based on fuzzy relations

**Module II :** **( 6 Hrs )**

Fuzzy Models: Mamdani , Sugeno, Tsukamoto

**Books:**

1. Neuro-Fuzzy and Soft Computing by S.R.Jung, Sun, Mizutani,

**604203B                      Design and Analysis of Algorithm (Elective III)**

**Credits:2**

**Teaching Scheme:**

**Lectures: 2 Hrs/Week**

**Examination Scheme\*:**

**In-Sem                      : 50 Marks**

**End-Sem                    : 50 Marks**

**Module I :**

**( 8 Hrs )**

Introduction- Fundamental characteristics of an algorithm. Basic algorithm analysis – Asymptotic analysis of complexity bounds– best, average and worst-case behaviour, standard notations for expressing algorithmic complexity. Empirical measurements of performance, time and space trade-offs in algorithms.

**Module II :**

**( 8 Hrs )**

Properties of big-Oh notation – Recurrence equations – Solving recurrence equations – Analysis of linear search. Divide and Conquer: General Method – Binary Search – Finding Maximum and Minimum – Merge Sort – Greedy Algorithms: General Method – Container Loading – Knapsack

**Books:**

Algorithm Design – Jon Kleinberg and Eva Tardos Introduction to Algorithms – T.H. Corman

**604103**

**CUDA  
ELECTIVE- III B**

**Group II**

**Teaching Scheme:**  
**Lectures 2 Hrs/ Week**

**Examination Scheme:**  
**Theory : 50 Marks (In Semester)**  
**50 Marks (End Semester)**  
**Credits : 2**

**Module I :**

History of GPUs leading to their use and design for HPC- The Age of Parallel Processing, The Rise of GPU Computing ,CUDA, Applications of CUDA, Development Environment, Introduction to CUDA C, Kernel call, Passing Parameters, Querying Devices, Using Device Properties

**Module II:**

Parallel Programming in CUDA C - CUDA Parallel Programming, Splitting Parallel Blocks, Shared Memory and Synchronization, Constant Memory, Texture Memory, CUDA events, Measuring Performance with Events.

**Books:**

1. Programming Massively Parallel Processors: A Hands-on Approach –second edition by David B. Kirk, Wen-mei W. Hwu.
2. CUDA by Example - An Introduction to General-Purpose GPU Programming by Jason Sanders ,Edward Kandrot- Addison Wesley
3. GPU Computing Gems Emerald Edition -Applications of GPU Computing Series by Wen-mei, W. Hwu
4. CUDA Programming: A Developer's Guide to Parallel Computing with GPUs by shane cook

**604204**

**Seminar II**

**Credits:4**

**Teaching Scheme:**

**4 Hrs/Week**

**Examination Scheme:**

**Term Work : 50 Marks**

**Oral/ Presentation: 50 Marks**

**Seminar II** : shall be on the topic relevant to latest trends in the field of concerned branch, preferably on the topic of specialization based on the electives selected by him/her approved by authority. The student shall submit the seminar report in standard format, duly certified for satisfactory completion of the work by the concerned guide and head of the Department/Institute.



604205

**Project Stage- I**  
**Credits: 8**

**Teaching Scheme:**

**Lecture : 8 Hrs/week**

**Examination Scheme:**

**Term Work : 50 Marks**  
**Oral : 50 Marks**

**Project Stage – I**

Project Stage – I is an integral part of the project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation (Mathematical Model/SRS/UML/ERD/block diagram/PERT chart, etc.) and Layout & Design of the Set-up. As a part of the progress report of Project work Stage-I, the candidate shall deliver a presentation on the advancement in Technology pertaining to the selected dissertation topic.

The student shall submit the duly certified progress report of Project work Stage-I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

604206

**Seminar III**  
**Credits: 5**

**Teaching Scheme:**

**Lectures : 5 Hrs/week**

**Examination Scheme:**

**Term Work : 50 Marks**

**Oral/ : 50 Marks**

**Presentation**

Seminar III shall preferably be an extension of **seminar II**. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

604207

**Project Stage- II**  
**Credits: 20**

**Teaching Scheme:**

**Lecture : 20 Hrs/week**

**Examination Scheme:**

**Term Work : 150 Marks**  
**Oral : 50 Marks**

In Project Stage – II, the student shall complete the remaining part of the project which will consist of the fabrication of set up required for the project, work station, conducting experiments and taking results, analysis & validation of results and conclusions.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.