K.K.Wagh Institute of Engineering Education and Research, Nashik (Autonomous w.e.f. A.Y.2022-23)

Department of Electronics and Telecommunication Engineering

Details of Course Structure: Semester - I F.Y.M.Tech (VLSI and Embedded System)

Course Code	Course Type	Title of Course	Teaching Scheme Hrs./week			Assessment Scheme and Marks						Credits			
			TH	TU	PR	In Sem	End Sem	CA	TU/ TW	PR/ OR	Total	TH	TU / TW	PR/ OR	Total
ETC225101	DCC	F1: Embedded Product Design	3	-	-	20	60	20	-	-	100	3	-	-	3
ETC225102	DCC	F2: ASIC Design	3	-	-	20	60	20	-	-	100	3	-	-	3
ETC225103	DCC	F3: VLSI Design Verification and Testing	3	-	-	20	60	20	-	-	100	3	-	-	3
ETC225104	DEC	**F4: Elective 1** A: Linux in Embedded System B: Static Timing Analysis C: MEMS and Microsystem Design	3	-	-	20	60	20	-	-	100	3	-	-	3
ETC225105	LH SM	F5 : Research Methodology and IPR	3	-	-	20	60	20			100	3	-	-	3
ETC225106	DCC	F6: Lab. Practice I	-	-	4	-	-	-	25	25	50	-	-	2	2
		Total	**15**	**-**	**4**	**100**	**300**	**100**	**25**	**25**	**550**	**15**	**-**	**2**	**17**

K.K.Wagh Institute of Engineering Education and Research, Nashik (Autonomous w.e.f. A.Y.2022-23)

Department of Electronics and Telecommunication Engineering

Details of Course Structure: Semester -II F.Y.M.Tech (VLSI and Embedded System)

Course Code	Course Type	Title of Course	Teaching Scheme Hrs./week			Assessment Scheme and Marks						Credits			
			TH	TU	PR	In Sem	End Sem	CA	TU/ TW	PR/ OR	Total	TH	TU / TW	PR/ OR	Total
ETC225107	DCC	F7: Real Time Embedded System	3		-	20	60	20	-	-	100	3	-	-	3
ETC225108	DCC	F8: ML in Chip Design	3		-	20	60	20	-	-	100	3	-	-	3
ETC225109	DCC	F9: VLSI for AI & Neural Networks	3		-	20	60	20	-	-	100	3	-	-	3
ETC225110	DEC	**F10: Elective II** A: Embedded Computing and Networking B: VLSI Architectures for DSP C: Advanced IoT Applications	3		-	20	60	20	-	-	100	3	-	-	3
ETC225111	DCC	F11: Lab. Practice II	-		4	-	-	-	25	25	50	-	-	2	2
ETC225112	PSI	F12: Seminar1	-		4	-	-	-	25	25	50	-	-	2	2
ETC225113	IMC	F13: Software application for professional skill upgradation (LATEX, Power Point &Excel)	-		4			25		25	50	-	-	2	2
		Total	**12**		**12**	**80**	**240**	**105**	**50**	**75**	**550**	**12**	**-**	**6**	**18**

K.K.Wagh Institute of Engineering Education and Research, Nashik (Autonomous w.e.f. A.Y.2022-23)

Department of Electronics and Telecommunication Engineering

Details of Course Structure: Semester – III S.Y.M.Tech (VLSI and Embedded System)

Course Code	Course Type	Title of Course	Teaching Scheme Hrs./week			Assessment Scheme and Marks						Credits			
			TH	TU	PR	In Sem	End Sem	CA	TU/ TW	PR/ OR	Total	TH	TU / TW	PR/ OR	Total
ETC226101	DEC	**S1:Elective III** A:Communication Buses and standards B:Automotive embedded Product Development C:Embedded Systems Security	3		-	20	60	20	-	-	100	3	-	-	3
ETC226102	LHSM	S2: Indian Constitution	2		-	-	25	25	-	-	50*	2	-	-	2
ETC226103	PSI	S3: Dissertation Phase-1	-		20	-	-	50	50	50	150	-	-	10	10
ETC226104	IMC	S4: Internship Seminar 2	-		4	-	-	-	25	25	50	-	-	2	2
		Total	**5**		**24**	**20**	**85**	**95**	**75**	**75**	**350**	**5**	**-**	**12**	**17**

*Assessment/evaluation shall be done for 100 marks which must be converted to 50 marks as per structure.

S4 will be seminar on internship and report submission. The internship of minimum 4 weeks is required to be done during the vacation after 2nd semester

K.K.Wagh Institute of Engineering Education and Research, Nashik(Autonomous w.e.f. A.Y.2022-23)

Department of Electronics and Telecommunication Engineering

Details of Course Structure:Semester - IV S.Y.B.Tech (Group B)

Course Code	Course Type	Title of Course	Teaching Scheme Hrs./week			Assessment Scheme and Marks						Credits			
			TH	TU	PR	In Sem	End Sem	CA	TU/ TW	PR/ OR	Total	TH	TU / TW	PR/ OR	Total
ETC226105	MOOCS	S5:MOOCs/NPTEL	-		-	--	100*	-	-	-	100	3	-	-	3
ETC226106	PSI	S6: Dissertation Phase-II	-		30	--	-	50	100	100	250	-	-	15	15
		Total			**30**	**-**	**-**	**50**	**100**	**100**	**250**	**3**	**-**	**15**	**18**

For S5 (MOOCs/NPTEL), students shall enroll for the MOOCs/NPTEL course in third semester and its evaluation shall be considered in the fourth semester. A course of minimum 8 weeks is mandatory.

For S5 (MOOCS/NPTEL), students can choose subjects from the following list

A: Parallel Computing
B: SOC Verification using System Verilog
C: Introduction to Embedded Systems Software and Development Environments
D: Introduction to Embedded Machine Learning
E: Introduction to FPGA Design for Embedded Systems
F: Courses based on advanced topics as per recommendations from BOS based on available courses in relevant semester.

K. K. Wagh Institute of Engineering Education and Research, Nashik
Department of Electronics and Telecommunication Engineering
(Autonomous from Academic Year 2022-23)

F. Y. M. Tech.(VLSI and Embedded System)
Pattern 2022 Semester: I
ETC225101 **:** Embedded Product Design

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week **Practical :--**	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks** **TermWork: -**

Prerequisite Courses, if any: Semiconductor Theory, Mathematics

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Find specifications and design challenges of embedded products	Applying
CO2	Estimate cost of embedded product	Understanding
CO3	Understand the aspects of Mechanical Packaging, Testing, reliability and failure analysis, EMI/RFI Certification and Documentation	Understanding
CO4	Demonstrate the knowledge of embedded product design related hardware and software design tools	Applying
CO5	Learn all aspects of an applications and it improves the quality of a product.	Remembering

COURSE CONTENTS

Unit I	**Overview of Embedded Products**	**(08hrs)**	**COs Mapped – CO1**

Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components, Iteration and refinement of the partitioning.

Unit II	**Design Models and Techniques**	**(07hrs)**	**COs Mapped – CO2**

Various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology.

Unit III	**Hardware and Software Modules**	**(07hrs)**	**COs Mapped – CO3**

Trade offs, Custom Single-purpose processors, General purpose processors, Software, Memory, Interfacing, Design technology-Hardware design, FPGA design, firmware design, driver development

Unit IV	Testing and verification	(07hrs)	COs Mapped – CO4
Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion.			
Unit V	**Documentation**	**(07hrs)**	**COs Mapped – CO5**
Mechanical Packaging, Testing, reliability and failure analysis, communication protocols, Certification (EMI/ RFI) and its documentation. Study of any two real life embedded products in detail.			

Text Books

1. "Embedded System Design" by Marwedel P, Springer Publication

Reference Books

1. "Embedded System Design: A Unified Hardware/Software Introduction" by Vahid Frankand Tony Givargis, Student Edition, John Wiley Publication
2. "Embedded Systems – A Contemporary Design Tool" by James K. Peckol, Wiley publication

	Strength of CO-PO/PSO Mapping							
	PO						PSO	
	1	2	3	4	5	6	1	2
CO1	3	-	2	-	-	-	-	-
CO2	3	-	2	-	-	-	-	-
CO3	3	-	2	-	-	-	2	-
CO4	3	-	-	3	-	-	2	-
CO5	3	3	-	-	-	-	-	-

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K. K. Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech. (VLSI and Embedded System)

Pattern 2022 Semester: I

ETC 225102: ASIC Design

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week **Practical :**	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks** **TermWork: -**

Prerequisite Courses, if any: Semiconductor Theory, Mathematics

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Illustrate the idea of ASIC, Data logic cells	Understanding
CO2	Explore knowledge of ASIC design flow along with programmable ASIC interconnect.	Understanding
CO3	Discuss about low level design in ASIC construction.	Applying
CO4	Understand issues and tools related to ASIC/FPGA design and implementation	Applying
CO5	Apply ASIC construction floor planning and placement and routing	Analyzing

COURSE CONTENTS

Unit I	**Introduction to ASICs**	**(07hrs)**	**COs Mapped – CO1**

Types of ASICs , Design flow , Economics of ASICs , ASIC cell libraries , CMOS logic cell data path logic cells , I/O cells – cell compilers.

Unit II	**ASIC design**	**(08hrs)**	**COs Mapped – CO2**

ASIC Library design: Transistors as resistors , parasitic capacitance , logical effort Programmable ASIC design software: Design system, logic synthesis, half gate ASIC.

Unit III	**Low level design entry:**	**(08hrs)**	**COs Mapped – CO3**

Schematic entry. low level design languages, PLA tools, EDIF, overview of VHDL and Verilog

Unit IV	**Logic synthesis and Testing**	**(08hrs)**	**COs Mapped – CO4**

Logic synthesis in Verilog and & VHDL simulation and Testing

Unit V	**ASIC Construction**	**(08hrs)**	**COs Mapped – CO5**

Floor planning & placement, Routing ,Low power VLSI design techniques, Technology Challenges

Text Books

1. "Application specific Integrated Circuits", J.S. Smith, Addison Wesley.
2. "Principles of CMOS VLSI Design : A System Perspective", N. Westle & K. Eshraghian ,Addison – Wesley Pub.Co.1985.

Reference Books

1. Basic VLSI Design :Systems and Circuits, Douglas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd. , New Delhi , 1989.
2. Introduction to VLSI System,C. Mead & L. Canway, Addison Wesley Pub
3. Introduction to NMOS & VLSI System Design, A. Mukharjee, Prentice Hall
4. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
5. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: I

ETC 225103: VLSI Design Verification and Testing

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: UG Courses on Digital Electronics and VLSI Design & Technology

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Understand basics of modeling and simulation.	Understanding
CO2	Identify and model fault.	Understanding
CO3	Apply compression technique and understand the self-checking system.	Applying
CO4	Understand design for testability.	Understanding
CO5	Understand system testing & core based design.	Understanding

COURSE CONTENTS

Unit I	**Modeling and Logic Simulation:**	**(07hrs)**	**COs Mapped – CO1**

Functional modeling at the logic and the register level, Structural models, Level of modeling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation, different delay models, Hazard Detection.

Unit II	**Fault Modeling and Fault Simulation:**	**(08hrs)**	**COs Mapped – CO2**

Logical fault models, Fault detection and Redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, Multiple stuck fault model, stuck RTL variables, Fault variables. Testing for single stuck fault and Bridging fault, General fault simulation techniques, Serial and Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis.

Unit III	**Compression techniques and Self checking System:**	**(07hrs)**	**COs Mapped – CO3**

General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis, Self checking Design, Multiple – Bit Errors, self– checking checkers, Parity – check function , totally self-checking m/n code checkers, totally self-checking equality checkers, Self-checking Berger code checkers and self checking combinational circuits.

Unit IV	Design for testability	(07hrs)	COs Mapped – CO4
Scan and Boundary scan architectures, JTAG, Built-in Self-test (BIST) and current-based testing, analog test bus standard.			
Unit V	**System test and core-based design**	**(07hrs)**	**COs Mapped – CO5**
ATPG, Embedded core test fundamentals. Design verification techniques based on simulation, analytical and formal approaches,Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.			

Text Books

1. "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", by Bushnell M L, Agrawal V D, Kluwer Academic Publishers
2. "Digital systems and Testable Design" by, Abramovici M, Breuer M A and FriedmanA D, Jaico Publications

Reference Books

1. "Design Test for Digital IC's and Embedded Core Systems" by Crouch A L, Prentice Hall\
2. "Introduction to Formal Hardware Verification" by Kropf T, Springer Publications

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech.(VLSI and Embedded System)
Pattern 2022 Semester: I
ETC225101: Linux in Embedded system(Elective I)

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: Embedded System

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Create complex applications with multiple processes and threads incorporating synchronization and inter-process communication features	Applying
CO2	Understand kernel basics	Understanding
CO3	Recognize the standard Linux and Embedded file systems and emulate simple tasks based on the file system.	Applying
CO4	Development Interrupt management system using ARM	Applying
CO5	Understand embedded Linux development model.	Understanding

COURSE CONTENTS

Unit I	Linux OS Introduction:	**(08hrs)**	**COs Mapped – CO1**

User/Kernel Model, Processes, Daemons, Threads, System Calls, Shell, Shell, Virtual Memory. Executable file layout User Level Programming: Creating Processes, Linking/Loading, Signals, Shared Library, Threads and multithreaded program, Semaphores, Mutex, IPC mechanism Pipes, Shared memory.

Unit II	Kernel Internals Basics:	**(08hrs)**	**COs Mapped – CO2**

Process Internal representation, Linux File System Abstraction, Virtual File system, iNodes, files, /proc, Kernel Queue Data Structure, Memory Allocation (buddy system, slab cache), Embedded File systems

Unit III	Working with Kernel Artifacts:	**(08hrs)**	**COs Mapped – CO3**

Kernel Layers, Basic Driver Architecture,Device drivers, Kernel configuration.Block & character driver distinction, Low level drivers, OS drivers etc, Device major, minor number, Interfaces to driver read, write, ioctl etc, Blocking and non-blocking calls, Semaphores, Mutex Multi core Synchronization, and spin locks, Proc & Sysfs interfaces, Block driver examples, BIOS versus boot-loader, Booting the kernel

Unit IV	Interrupt Management:	**(08hrs)**	**COs Mapped – CO4**
Interrupt Handling in Normal Processor, Traditional ARM7 multi mode interrupts, Interrupt Control Mechanism, Interrupts and bottom halves, Writing interrupt driven drivers, Implementing bottom halves, Kernel Threads & Work Queues, Kernel timer, Jiffies, Timer interrupts			
Unit V	Linux Control Groups and TCP/IP Networking:	**(08hrs)**	**COs Mapped – CO5**
Resource limiting, Prioritization, Accounting and Control, Sockets APIs, Client and Server design, Remote Procedure Call Embedded Linux Specific: Boot sequence, I2C, SPI driver structure and application, Study of Simulated PCI driver, Linux Kernel Structure, BSP.			

Text Books

1. "Embedded Linux Primer: A Practical Real World Approach" by Christopher Hallinan, Wiley, Ninth Edition

Reference Books

1. "Operating System Concepts" by Abraham Silberschatz, Peter B. Galvin, Greg Gagne, Wiley, Ninth Edition
2. "Linux Device Drivers" by Jonathan Corbet, Alessandro Rubini, O'Reilly, Third Edition
3. "Building Embedded Linux Systems" by KarimYaghmour, O'Reilly & Associates

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**

1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech. (VLSI and Embedded System)

Pattern 2022 Semester: I

ETC225104**: Static Time Analysis**

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week **Practical :-**	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks** **TermWork: 25Marks**

Prerequisite Courses, if any: Semiconductor Theory, Mathematics

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Understand the basics of Static time analysis	Understanding
CO2	Explain what static timing analysis is and how it is used for timing verification	Understanding
CO3	Explain timing terminology related to static timing analysis	Understanding
CO4	Explain various techniques for modelling and representing interconnect parasitic and cell delays and paths delays are compute.	Applying
CO5	Explain various methods for specifying clocks, IO characteristics, false paths and multicycle paths	Applying

COURSE CONTENTS

Unit I	**Introduction to Static Time Analysis(STA):**	**(07hrs)**	**COs Mapped – CO1**

What is Static Timing Analysis (STA)? STA vs DTA, STA vs SPICE , Advantages of Static Timing Analysis, Disadvantages of Static Timing Analysis STA Flow, Inputs to STA Flow, STA Tools

Unit II	**STA Concepts:** CMOS Logic Design.	**(08hrs)**	**COs Mapped – CO2**

Modelling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unsafeness, Min and Max Timing Paths, Clock

Unit III	**Timing Modelling and Analysis :**	**(08hrs)**	**COs Mapped – CO3**

Linear Timing Model, Non-Linear Delay Model, Timing Models - Combinational Cells, Timing Models - Sequential Cells ,State-Dependent Models, Advanced Timing Modeling.

Unit IV	**Interconnect Parasitic sand Delay Calculation :**	**(08hrs)**	**COs Mapped – CO4**
RLC for Interconnect, Wire load Models, Reducing Parasitic for Critical Nets, Delay Calculation Basics ,Delay Calculation with Interconnect, Interconnect Delay, Path Delay Calculation			
Unit V	**Configuring the STA Environment:**	**(08hrs)**	**COs Mapped – CO5**
What is the STA Environment? Specifying Clocks, Generated Clocks, Constraining Input Paths and Output Paths, Timing Path Groups, Design Rule Checks, Refining the Timing Analysis, Path Segmentation			

Text Books

1. Static Timing Analysis for Nanometer Designsby J. Bhasker Rakesh Chadha Springer

Reference Books

1. Fundamentals of digital circuits by A.Anand Kumar, 2nd Edition,PHIPublishers
2. Digital Design by M. Morris Mano, 4th edition,PHI Publishers

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

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F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: I

ETC 225104: Elective 1 MEMS and Microsystem Design

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: UG Courses on Digital Electronics and VLSI Design & Technology

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Understand basics of MEMS and microsystems.	Understanding
CO2	Study working principle of MEMS and microsystems.	Understanding
CO3	Explore materials used for MEMS and Microsystems	Understanding
CO4	Explore fabrication techniques used for MEMS and Microsystems	Understanding
CO5	Design electronic circuits for MEMS and Microsystems	Designing

COURSE CONTENTS

Unit I	**Overview of MEMS and Microsystems**	**(05hrs)**	**COs Mapped – CO1**

Introduction to MEMS and Microsystems, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microelectronics and Microsystems, Applications of MEMS

Unit II	**Working Principles of MEMS and Microsystems**	**(07hrs)**	**COs Mapped – CO2**

Introduction to Microsensors and Microactuators, Sensing techniques for MEMS: Piezoresistive, Piezoelectric, Capacitive and Optical sensing methods, Microactuation techniques for MEMS: Actuation methods using Thermal forces, Piezoelectric crystals and Electrostatic forces, Examples of MEMS based Microsensors and Microactuators.

Unit III	**Materials for MEMS and Microsystems**	**(06hrs)**	**COs Mapped – CO3**

Materials**:** Substrates and Wafers, Active Substrate Materials, Silicon as a Substrate Material, Silicon Compounds, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers, Packaging Materials

Unit IV	**Fabrication Processes for MEMS and Microsystems**	**(06hrs)**	**COs Mapped – CO4**

Fabrication processes: Photolithography, Diffusion, Ion Implantation, Oxidation, Chemical Vapor Deposition, Physical Vapor Deposition – Sputtering, Deposition by Epitaxy, Dry and Wet Etching Techniques, Micromachining processes: Bulk and Surface Micromachining, The LIGA Process.

Unit V	Electronic circuits for MEMS and Microsystems	(06hrs)	COs Mapped – CO5
Semiconductor devices: Diodes, BJT, MOSFET, CMOS, Electronic Amplifiers, Operational amplifiers, Difference amplifier, Wheatstone Bridge circuit for measurement of resistance, Analog to Digital converter, Differential charge measurement, Switched capacitor circuits for capacitance measurement.			

Text Books

1. "MEMS and Microsystems: Design and Manufacture", T.R. Hsu, McGraw Hill
2. "Analysis and Design Principles of MEMS Devices", H. Bao, Elsevier

Reference Books

1. "Fundamentals of Microfabrication: The Science of Miniaturization", M. J. Madou, CRC Press
2. "Micro and Smart Systems", G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat and V.K. Aatre, Wiley India
3. "Microsystem Design", S.D. Senturia, Springer

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

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F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: I

ETC225105 : Research Methodology and IPR

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: NA

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Conduct a quality literature review and find the research gap.	Understanding
CO2	Identify an original and relevant problem and identify methods to find its solution.	Understanding
CO3	Analyze strategy of experimentation, statistics for modeling and performance prediction	Analyzing
CO4	Explain concept of Hypethesis	Understanding
CO5	Discuss research ethics and Understand IPR protection for further research and better products.	Understanding

COURSE CONTENTS

Unit I	**Research techniques vs. Methodology**	**(08hrs)**	**COs Mapped – CO1, CO12**

Research techniques vs. Methodology – Motivation and goals, Types of analysis – Descriptive vs. Analytical, Applied vs. Fundamental, Quantitative vs. Qualitative, Conceptual vs. Empirical, concept of applied and basic research process, criteria of good research,

Literature review:-Primary and secondary sources, reviews, monographs, patents, research databases, the web as a source, web searching, critical literature review, finding gaps in the literature and research database, creation of working hypothesis

Defining and formulating the research problem:- choosing the problem, the importance of defining the problem, and the importance of conducting a literature review in problem definition,

Research process: eight step model - formulating research problem, conceptualizing research design, constructing instrument for data collection, Selecting a sample, writing a research proposal, collecting data, processing data, writing research report.

Unit II	**Design of Experiments**	**(08hrs)**	**COs Mapped - CO1, CO12**

Taguchi Method to plan a set of experiments or simulations or build prototype, analyze your results and draw conclusions or Build Prototype, Test and Redesign, analysis Plagiarism, Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Techniques, Multidimensional Scaling, Deciding the Scale.
Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

Unit III	**Strategy of Experimentation**	**(08hrs)**	**COs Mapped – CO1, CO12**

Strategy of Experimentation - Typical applications of experimental design - Guidelines for designing experiments - Basic statistical concepts - Statistical concepts in experimentation - Regression approach to analysis of variance.
Applied Statistics: Regression analysis, Parameter estimation, Multivariate statistics, Principal component analysis, Moments and response curve methods, State vector machines and uncertainty analysis.
Modeling and prediction of performance: Setting up a computing model to predict performance of experimental system, Multi-scale modeling and verifying performance of process system, Nonlinear analysis of system and asymptotic analysis, Verifying if assumptions hold true for a given apparatus setup, Plotting family of performance curves to study trends and tendencies, Sensitivity theory and applications.
Computer and its role in research, Use of statistical software SPSS, GRETL, etc. in research.
Introduction to evolutionary algorithms - Fundamentals of Genetic algorithms, Simulated Annealing, Neural Network based optimization, Optimization of fuzzy systems.

Unit IV	**Hypothesis**	**(08hrs)**	**COs Mapped – CO1, CO12**

Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis. Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, and Cautions in Using Chi Square Tests

Unit V	**Intellectual Property**	**(08hrs)**	**COs Mapped – CO1, CO12**

Intellectual Property: IPR- intellectual property rights and patent law, commercialization, copy right, royalty, trade related aspects of intellectual property rights (TRIPS); scholarly publishing- IMRAD concept and design of research paper, citation and acknowledgement, plagiarism, reproducibility and accountability.
Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.

Text Books

1. An Introduction to Research Methodology, RBSA Publishers, Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002
2. Research Methodology: A Step by Step Guide for Beginners, Second edition, SAGE Publications Ltd 3rd Edition, 2011, Ranjit Kumar
3. Research Methodology: Methods and Trends, New Age International 4th Edition, 2018, Dr. Kothari C R

Reference Books

1. Research methodology: An Introduction for Science & Engineering students , Melville Stuart, Goddard Wayne
2. Methods: the concise knowledge base, Trochim Atomic Dog Publishing

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech. **Pattern 2022 Semester: I** **ETC225107:** Lab Practice I		
Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :- **Practical : 04 hrs/week**	**02**	**OR:25Marks** **Term Work: 25Marks**

The laboratory work will be based on completion of minimum two assignments/experiments confined to the following courses of that first semester

A. Embedded Product Design
B. VLSI Design Verification and Testing
C. Elective I Linux in Embedded System
D. Elective I MEMS and Microsystem Design
E. ASIC Design
F. Elective I Static Time Analysis

A. Embedded Product Design

Group of Course: DCC

Prerequisites for the course: Embedded System Design

Course Objectives and Outcomes:

Course Outcomes	Description After successful completion of the course students will be able to	Bloom's Level
CO1	Demonstrate the knowledge of embedded product design related hardware and software design tools	Applying
CO2	Understand the aspects of Testing and estimate cost of embedded product	Understanding

List of Experiments:

Unit No.	Contents	CO mapped
1	Estimate techno-commercial feasibility of any one embedded product such as mobile phone, programmable calculator, tablet PC, set top box etc.	**CO1**
2	Study of design considerations of any one embedded product.	**CO1**
3	Design any one embedded product to solve any real life problems. Estimate cost of embedded product	**CO1**
4	Simulate the software and test the hardware designed for above assignment (3) using suitable simulation tool.	**CO2**
5	Develop Hardware for assignment 3. Select the Microcontroller, Memory and peripherals. Design the enclosure for the system. Test the hardware using emulator	**CO1,CO2**

CO-PO Mapping

B. VLSI Design Verification and Testing

Prerequisites for the course: VLSI Design Verification and Testing

Course Objectives and Outcomes:

Course Outcomes	Description On completion of the course, student will be able to,	Bloom's Level

CO1	Implement modelling and simulation technique for fault detection.	Applying
CO2	Implement and analyse various compression technique.	Applying

List of Experiments:

Sr. No.	Contents	CO mapped
1	Simulate a single input signature analyser for given characteristic equation and input sequence.	**CO1**
2	Implement different compression techniques like ones- count, transition- count.	**CO2**
3	Implement a self-checking system in automatic detection of fault.	**CO1**
4	Implement different fault models using back end tools.	**CO1**
5	Design event driven simulation model using VLSI simulation software.	**CO1**

CO-PO Mapping

	Strength of CO-PO/PSO Mapping							
	POs						**PSOs**	
	1	**2**	**3**	**4**	**5**	**6**	**1**	**2**
CO1	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**
CO2	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**

C. Elective I - Linux in Embedded System

Group of Course: DEC

Prerequisites for the course: Embedded system

Course Objectives and Outcomes:

Course Outcomes	Description After successful completion of the course students will be able to	Bloom's Level
CO1	Develop multithreaded applications, libraries and device drivers for Linux OS	Applying
CO2	Configure, compile and load the embedded Linux kernel on to target platform.	Applying

Course context, Relevance, Practical Significance:

.**List of Experiments:**

Unit No.	Contents	CO mapped
1	Linux file systems and emulating several commands related to file systems such as ls, pwd	**CO1,CO2**
2	Develop and use pseudo and serial communication Linux device drivers	**CO1,CO2**
3	Design and implement custom network applications using socket programming	**CO1,CO2**
4	Compile and install bootloader and use basic commands of bootloader	**CO1,CO2**
5	Making a tiny embedded system with busy box	**CO1,CO2**

CO-PO Mapping

	Strength of CO-PO/PSO Mapping							
	PO						**PSO**	
	1	**2**	**3**	**4**	**5**	**6**	**1**	**2**
CO1	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**-**
CO2	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**-**

D. Elective1- MEMS and Microsystem Design

Prerequisites for the course: MEMS and Microsystem Design

Course Objectives and Outcomes:

Course Outcomes	Description On completion of the course, student will be able to,	Bloom's Level
CO1	Explore various MEMS components and sensors.	Understanding
CO2	Explore fabrication techniques used for MEMS and Microsystems	Understanding
CO3	Design electronic circuits for MEMS and Microsystems	Analysing

List of Experiments:

Sr. No.	Contents	CO mapped
1	To study and simulate a piezoresistive pressure sensor.	**CO1, CO3**
2	To study and simulate a capacitive pressure sensor.	**CO1, CO3**
3	To study and simulate a cantilever based resonator.	**CO1, CO3**
4	To study and simulate a beam based MEMS switch.	**CO1, CO3**
5	To study and develop MASKs for various MEMS devices.	**CO1, CO3**
6	To study and simulate various fabrication processes involved in the development of MEMS devices.	**CO2**

CO-PO Mapping

	Strength of CO-PO/PSO Mapping							
	POs						**PSOs**	
	1	**2**	**3**	**4**	**5**	**6**	**1**	**2**
CO1	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**
CO2	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**
CO3	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: II

ETC225107: Real Time Embedded System

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: Embedded System

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Study concepts of Real Time Embedded Systems	Understanding
CO2	Design real time embedded Systems	Analyzing
CO3	Interface Embedded system peripherals	Applying
CO4	Design of real time Embedded System Software	Analyzing
CO5	Do case study of real time embedded system	Analyzing

COURSE CONTENTS

Unit I	**Introduction:** I	**(08hrs)**	**COs Mapped – CO1**

ntroduction to Real Time Embedded Systems: design metrics of embedded system, Comparison of RealTime Embedded System from other systems, real and non-real time embedded system, components of embedded system

Unit II	**Embedded Systems design:**	**(07hrs)**	**COs Mapped – CO2**

Embedded Processors selection: Embedded processors and processor cores ARM, 486SX, Hitachi SH7000, NEC V800 Memory :Cache Memory - Different types of Cache Mappings, Performance Different types of Dynamic RAMs, shared Memory with multiprocessor, Memory Management Unit.

Unit III	**Embedded system peripherals**	**(07hrs)**	**COs Mapped – CO3**

Timers ,High speed I/O interfacing, AD and DA Converters, Embedded Communications Engineering, Universal Serial Bus Signals, IrDA standard, CAN, Ethernet, distributed embedded system.

Unit IV	**Design of real time Embedded, System Software:**	**(07hrs)**	**COs Mapped – CO4**

RTOS, Testing of Embedded System, Boundary Scan Methods and Standards

Unit V	**Case study of real time embedded system**	**(07hrs)**	**COs Mapped – CO5**

Mobile phone, Automatic cruise control system, Digital Camera, IOT application, real time, signal processing application
Text Books
1. "Embedded Microcomputer Systems: Real-Time Interfacing", Jonathan W. Valvano, Brookes/Cole, Pacific Grove, 2000.
Reference Books
1. "Embedded Systems Architecture, Programming and design" by Raj Kamal, Tata McGraw-Hill. 2. "Embedded / real time system" by Dr.K.V.K.K. Prasad, Dreamtech.

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

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F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: II

ETC225108: ML in Chip Design

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: VLSI Design

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Describe the Six categories of Artificial Intelligence	Understanding
CO2	Explain problem solving and Decision making applications	Applying
CO3	Explain machine learning for lithography and physical design	Understanding
CO4	Implement Machine Learning for VLSI Chip Testing and Semiconductor Manufacturing Process	Applying
CO5	Implement Fast Statistical Analysis Using Machine Learning	Applying

COURSE CONTENTS

Unit I	**Introduction to Artificial Intelligence and Machine Learning:** ,	**(07hrs)**	**COs Mapped – CO1**

Categories of Artificial Intelligence, The Six Macro Throughput Model Algorithms Driving Artificial Intelligence, Further Examination and Impact of Artificial Intelligence and Algorithms, Types of Expert Systems and Artificial Intelligence Systems, Machine learning: Basic concepts, How do we get machines to learn?

Unit II	**Artificial Intelligence Six Cognitive Driven Algorithms:**	**(08hrs)**	**COs Mapped – CO1, CO2**

Heuristics Used in Problem-Solving and Decision-Making, Six Dominant Algorithmic Pathways, Information Drives Implementing a Particular Algorithm

Unit III	**Machine Learning for Lithography and Physical Design:**	**(07hrs)**	**COs Mapped – CO3**

Machine Learning for Compact Lithographic Process Models, Machine Learning for Mask Synthesis, Machine Learning in Physical Verification, Mask Synthesis, and Physical Design

Unit IV	**Machine Learning for Manufacturing, Yield, and Reliability:**	**(07hrs)**	**COs Mapped – CO4**

Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications, Machine Learning Approaches for IC Manufacturing Yield Enhancement, Efficient Process Variation Characterization by Virtual Probe, Machine Learning for VLSI Chip Testing and Semiconductor Manufacturing Process Monitoring and Improvement, Machine Learning-Based Aging Analysis			
Unit V	**Machine Learning for Failure Modeling:**	**(07hrs)**	**COs Mapped – CO5**
Extreme Statistics in Memories, Fast Statistical Analysis Using Machine Learning, Fast Statistical Analysis of Rare Circuit Failure Events, Learning from Limited Data in VLSICAD			

Text Books

1. Artificial Intelligence in a Throughput Model Some Major Algorithms by Waymond Rodgers-CRC Press
2. Machine Learning in VLSI Computer-Aided Design by Ibrahim (Abe) M. Elfadel Duane S. Boning · Xin Li-Springer

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
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F. Y. M. Tech. (VLSI and Embedded System)

Pattern 2022 Semester: II

ETC225109: VLSI for AI & Neural Networks

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: Basic Knowledge of Artificial Intelligence and VLSI Design & Technology.

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Apply basic principles of AI	**Applying**
CO2	Analyze applications of AI techniques in intelligent agents using analog circuits	**Analyzing**
CO3	Demonstrate in intelligent agents, expert systems, artificial neural networks using VLSI techniques	**Applying**
CO4	Develop applications in an 'AI language', expert system shell, or data mining tool using multiprocessor.	**Applying**
CO5	Applying scientific method to models of machine learning.	**Applying**

COURSE CONTENTS

Unit I	**Overview of AI& Neural Network: -**	**(03hrs)**	**COs Mapped – CO1**

Introduction, hierarchical perspective and foundations, Problems of AI, AI techniques, Tic-Tac-Toe problem. Neural Network: Biological neurons and brain, mathematical models of neuron, basic structure of a neural network, Learning rules, ANN training, back propagation algorithm, Hopfield nets and application of Neural Network.

Unit II	**Analog Circuits for Neural Networks:**	**(03hrs)**	**COs Mapped – CO2**

AnalogVLSI Neural Learning Circuits, An Analog CMOS Implementation of Kohonen Network with learning capability, Back propagation learning Algorithms for Analog VLSI Implementation, An Analog Implementation of the Boltzmann machine with Programmable learning Algorithms, A VLSI Design of the minimum Entropy Neuron, A multi-layer Analog VLSI architecture for texture analysis Isomorphic to cortical cells in Mammalian Visual System

Unit III	**Digital Implementations of Neural Networks:**	**(03hrs)**	**COs Mapped – CO3**

A VLSI Pipelined Neuroemulator, A Low Latency Digital Neural Network Architecture, MANTRA: A multi-Model Neural-Network Computer, SPERT: A Neuro-Microprocessor, Design of Neural Self-Organization Chips for Semantic Applications, VLSI Implementation of a Digital Neural Network with Reward-Penalty Learning, Asynchronous VLSI Design For Neural System Implementation.

Unit IV	**Neural Networks on Multiprocessor Systems and Applications:**	**(03hrs)**	**COs Mapped – CO4**

VLSI-Implementation of Associative Memory Systems for Neural Information Processing, A Dataflow Approach for Neural Networks, A custom Associative chip used as a building block for a software reconfigurable multi-network simulator, Parallel Implementation of Neural Associative Memories on RISC processors, Reconfigurable Logic Implementation of memory-based neural networks: A case study of the CMAC network, cascadable VLSI Design for GENET, Parametrised into Hardware Neural network design and compilation, Knowledge processing in Neural Architecture, Two methods for solving Linear equations using Neural Networks.

Unit V	**VLSI Machines for Artificial Intelligence:**	**(03hrs)**	**COs Mapped – CO5**

Hardware support for data Parallelism in production Systems, SPACE: Symbolic Processing in Associative Computing Elements, PALM: A Logic Programming System on a Highly Parallel architecture, A Distributed parallel (DPAP) for the Execution of Logic Programs, Performance analysis of a parallel VLSI Architecture for Prolog, A Prolog VLSI System for Real Time Applications, An Extended WAM Based Architecture for OR-Parallel Prolog Execution, Architecture and VLSI Implantation of a Pegasus-II Prolog Processor.

Text Books

1. "Artificial Intelligence & Soft Computing" by Purva Raut,Dipali V.Koshti, Nikahat Mulla, Techno Knowledge publications.
2. "Neural Networks" by Satish Kumar, McGraw-Hill.
3. "Introduction to Artificial Neural Systems" by Jacek M. Zurada, Jaico Publishing House.
4. "Artificial Intelligence" by Saroj Kaushik, Cengage Learning

Reference Books

1. "VLSI for Neural Networks and Artificial Intelligence" by Jose G. Delgado-Frias W.R. Moore, Springer, Boston, MA.
2. "Artificial Intelligence and Machine Learning" by Chandra S.S.V, PHI.
3. "VLSI Artificial Neural Networks Engineering" by Elmasry, Mohamed I., Springer.
4. "Neural Networks and Learning Machines" by Simon O. Haykin, Pearson.

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
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F. Y. M. Tech. (VLSI and Embedded System)

Pattern 2022 Semester: II

ETC225110: Embedded Computing and Networking

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: Knowledge about microcontroller, embedded processors

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Interpret the embedded computing and illustrate instruction set for ARM processor and TI C55xx DSP processor.	Understanding
CO2	Analyze aspects of CPU with Performance and power consumption.	Analyzing
CO3	Categories two fundamental abstraction of a complex system on microprocessors: the process and the operating system.	Applying
CO4	Design a video accelerator with the use of multiprocessors.	Create
CO5	Elaborate networks used to build distributed embedded system.	Analyzing

COURSE CONTENTS

Unit I	Embedded Computing:	**(08hrs)**	**COs Mapped – CO1**

Introduction, complex systems and microprocessors, embedded system design process, formalism of system design, model train controller Instruction set: Computer architecture taxonomy, assembly language. ARM and TI DSP C55xx: Processor and memory organization, addressing modes, data operation and flow control.

Unit II	CPUs:	**(08hrs)**	**COs Mapped – CO2**

Programming I/O, supervisory, exception, trap, co-processors, memory system mechanism, CPU performance, CPU power consumption, design example: data compressor

Unit III	Processes and operating systems:performance, power management and optimization for processes, Design example: Telephone answering machine	**(08hrs)**	**COs Mapped – CO3**

Multiple task and multiple processes, preemptive real time operating systems, priority based scheduling, inter process communication mechanism, evaluating OS

Unit IV	Multiprocessors:	**(08hrs)**	**COs Mapped – CO4**
Why multiprocessors, CPUs and accelerators, multiprocessors performance analysis, consumer electronics architecture, Design example: cell phones, digital still cameras, video accelerators			
Unit V	Networks:	**(08hrs)**	**COs Mapped – CO5**
Distributed embedded architecture, networks for embedded system, network based design, internet-enabled system, vehicles as networks, design example: elevator controller			

Text Books

1. "Computers as Components Principles of Embedded Computing System Design" By Wayne Hendrix Wolf ,2005.
2. "Embedded Systems Architecture, Programming and Design" By Raj Kamal , 2011.

Reference Books

1. "Multiprocessing in Embedded Systems "by K. C. Wang.
2. "Architecting High-Performance Embedded Systems: Design and build high-performance real-time digital systems based on FPGAs and custom circuits" by Jim Ledin.

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**

2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

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F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: I

ETC225110: VLSI Architectures for DSP

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: DSP, VLSI, Mathematics.

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Understand the essential features of controller architectures and find which can be incorporated in VLSI chip	**Understanding**
CO2	Implementation of data path and control path	**Applying**
CO3	Understand pipelining and model it using HDL	**Applying**
CO4	Understand important building blocks related to highly accurate computation	**Understanding**
CO5	Study architectures for programmable digital signal processing devices	**Understanding**

COURSE CONTENTS

Unit I	**Instruction set architectures and performance control**	**(8hrs)**	**COs Mapped – CO1**

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI chips CISC Instruction-set implementation and RT-Level optimization through hardware flow-charting (without/with pipelining concepts) Handling of Instruction boundary interrupts, Immediate interrupts and traps in processors Assessing understanding performance: Overview CPU performance and its factors, evaluating performance, real stuff: Two spec benchmarks and performance of recent INTEL processors, fallacies and pitfalls

Unit II	**Data path-control and Computational accuracy in DSP implementations:**	**(8hrs)**	**COs Mapped -** CO2

Introduction, logic design conventions, building a data path - Simple implementation scheme, a multi cycle implementation, exceptions, Microprogramming approaches for implementation of control part of the processor: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors

Unit III	**Performance enhancement with Pipelining and Parallel Processing**	**(8hrs)**	**COs Mapped –** CO3
Introduction to Pipelining and Parallel processing - Merits and demerits of pipelined execution Pipelined data path, pipe lined control - Pipelined implementation of RISC Instruction Sets - Classic five stage pipeline for RISC processor Hazards of various types and pipeline stalling - Data hazards and forwarding, data hazards and stalls, branch hazards, using a hardware description language to describe and model a pipe line, exceptions Advanced pipelining: extracting more performance, fallacies and pitfalls			
Unit IV	**Instruction Level Parallelism - the Hardware Approach**	**(8hrs)**	**COs Mapped –** CO4
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach Branch prediction, high performance instruction delivery - hardware based speculation. ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.			
Unit V	**Architectures for programmable DSP devices:**	**(8hrs)**	**COs Mapped –** CO5
Introduction to VLSI Architectures - basic architectural features DSP computational building blocks - Implementation of DSP Instruction sets Programmable and function specific architectures, bus architecture and memory - data addressing capabilities, address generation unit, programmability and program execution - speed issues - features for external interfacing - Design of processing elements; Conventional, residue number, cordic and distributed arithmetic architectures			

Text Books

1. "VLSI Digital Signal Processing Systems: Design and Implementation", Keshab K. Parhi,Wiley publication.

Reference Books

1. "Digital signal processors" , B. Venkataramani and M. Bhaskar, Tata McGraw-Hill publication.

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**
2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

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F. Y. M. Tech.(VLSI and Embedded System)

Pattern 2022 Semester: II

ETC 225110: Advanced IoT Applications

Teaching Scheme:	Credit Scheme:	Examination Scheme:
Theory :03 hrs/week	**03**	**InSem Exam: 20Marks** **Continuous Assessment: 20Marks** **End Sem Exam: 60Marks**

Prerequisite Courses, if any: Knowledge on Programming, Problem Solving and embedded systems.

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	Bloom's Level
CO1	Illustrate IoT technologies, architectures, standards, and regulation.	Understanding
CO2	Interpret Cloud Computing and memorize the different Cloud service and deployment models.	Understanding
CO3	Explore the future of IOT for Health care applications.	Applying
CO4	Explore the future of IOT for Health care applications	Applying
CO5	Understand the fundamentals of various block Chain Techniques and Illustrate Challenge to Implementation of Blockchain in IoT	Applying

COURSE CONTENTS

Unit I	**Introduction to IoT**	**(08hrs)**	**COs Mapped – CO1**

Evolution of IoT ,IoT Architecture and Taxonomy ,Standardization Efforts , IoT Applications , Smart Home , Smart City , Smart Energy , Healthcare ,IoT Automotive ,Gaming, AR and VR ,Retail ,Wearable ,Smart Agriculture ,Industrial Internet ,Tactile Internet

Unit II	**Integration between Cloud Computing and Internet of Things (IoT) Technologies**	**(08hrs)**	**COs Mapped – CO2**

Cloud Computing Background ,Cloud Computing Models, Cloud Computing Infrastructure , Benefits of Cloud Computing ,IoT Background, IoT Devices and Connectivity , IoT Benefits and Applicability, Cloud Computing and IoT Integration,Challenges, Issues, and Implications

Unit III	**IoT in Healthcare**	**(08hrs)**	**COs Mapped – CO3**

Medicine and Technology, Information, Technology and Medicine ,Medical Equipment Technology, Remote Health Monitoring: Benefits of Remote Health Monitoring Challenges of Remote Health Monitoring Obstacles of Remote Health Monitoring Usage

Unit IV	"IoT" Bright Future in Healthcare Industry	(08hrs)	COs Mapped – CO4
Scope of IoT Information Accumulation, Device Integration, Real- Time Analytics, Apps and Method Abridgment, Healthcare Industry, Benefits of IoT in Healthcare Industry, Smart Pills, Smart Beds, App Integration. Technology of Smart Bed, Smart Wearable, Remote Health Monitoring, IOT- Enabled Applications			
Unit V	**Blockchain in IoT Technologies**	**(08hrs)**	**COs Mapped – CO5**
Blockchain: An Overview, Generations of Blockchain --Blockchain 1.0: Bitcoin and Cryptocurrency , Blockchain 2.0: Smart Contracts and Ethereum , Blockchain 3.0: Convergence toward Decentralized Applications, Blockchain 4.0: Seamless Integration with Industry 4.0, IoT Architecture and Systemic Challenges , Challenge to Implementation of Blockchain in IoT, Application of Blockchain in IoT Sector			

Text Books

1. "Introduction of IOT" by Sudip Misra, Anandarup Mukherjee, Arijit Roy, Cambridge university press.
2. "Cloud Security and Privacy: An Enterprise Perspective on Risks and Compliance" Tim Mather, Subra Kumaraswamy, ShahedLatif, O'Reilly Media; 1 edition 2009
3. "Block Chain & Crypto Currencies" Anshul Kaushik, , Khanna Publishing House

Reference Books

1. "Internet of Things (A Hands-on-Approach)", Vijay Madisetti and ArshdeepBahga, 1st Edition, VPT, 2014
2. "Cloud Computing Bible", Barrie Sosinsky, Wiley-India, 2010
3. "Mastering Blockchain: Deeper insights into decentralization, cryptography, Bitcoin, and popular Blockchain frameworks" Imran Bashir, Packt Publishing (2017).

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** Assignment No. 1 - Unit 1, 2 (10 Marks) Assignment No. 2 - Unit 3, 4, 5 (10 Marks)	**20**

2	**Test** Test 1 (15 Marks) Test 2 (15 Marks)	**20**

K.K.Wagh Institute of Engineering Education and Research, Nashik

Department of Electronics and Telecommunication Engineering

(Autonomous from Academic Year 2022-23)

F. Y. M. Tech.(VLSI and Embedded System) **Pattern 2022 Semester: II** **ETC225111: Lab Practice II**		
Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Practical : 04 hrs/week	**02**	**OR: 25Marks** **Term Work: 25Marks**

The laboratory work will be based on completion of minimum two assignments/experiments confined to the following courses of that semester

A. Real Time Embedded Systems
B. ML in Chip Design
C. Elective II Embedded Computing and Networking
D. Elective II VLSI Architectures for DSP
E. Elective II Advanced IoT Applications
F. VLSI for AI & Neural Network

A. Real Time Embedded Systems

List of Experiments:

Unit	**Content**	**CO Mapped**
1	Design a automotive cruise control system monitoring different parameters of vehicle	**CO1,CO2**
2	Design a data acquisition system using RTOS using 10 sensors. System will be touch screen based	**CO1,CO2**
3	Develop embedded system require for IOT application	**CO1,CO2**
4	Develop embedded system for signal processing application. Use open source IDE for software development	**CO1,CO2**
5	Test the real time embedded system using open source software	**CO1,CO2**

	Strength of CO-PO/PSO Mapping							
	PO						PSO	
	1	2	3	4	5	6	1	2
CO1	3		3	2	-	-	-	-
CO2	3		3	2	-	-	-	-

B.ML in Chip Design

CourseOutcomes:

Course Outcomes	Description After successful completion of the course students will be able to
CO1	Understand the implementation procedures for the machine learning algorithms.
CO2	Identify and apply Artificial Intelligence to solve real world problems.

List of Experiments:

Unit No.	Contents	CO mapped
1	Plot neuron output over the range of inputs	CO1
2	Classification of linearly separable data with a perceptron	CO2
3	AI with Python – Supervised Learning: Classification	CO2
4	Write a program to construct a Bayesian network considering medical data. Use this model to demonstrate the diagnosis of heart patients using standard Heart Disease Data Set. You can use Java/Python ML library classes/API.	CO1
5.	Implement signal processing system on system on Chip	CO2

CO-PO Mapping for Practical

C: ElectiveII Embedded Computing and Networking

Course Outcomes:

Course Outcomes	Description On completion of the course, student will be able to,
CO1	Illustrate instruction set for ARM processor and TI C55xx DSP processor
CO2	Implement various addressing modes of CPU for TI C55XX
CO3	Implement concept of operating system used for TI C55XX

List of Experiments:

Sr. No.	Contents	CO mapped
1	To study and simulate the instruction set for ARM 11.	**CO1**
2	To study and simulate the instruction set for TI C55XX	**CO1, CO2**
3	Implement various addressing modes for TI C55XX and compare.	**CO1, CO2**
4	Implement inter process communication in RTOS on TI C55XX	**CO1, CO2, CO3**
5	Implement task scheduling in RTOS on TI C55XX	**CO1, CO2, CO3**
6	Case study: Design of cell phones and digital still cameras	**CO1, CO2, CO3**

CO-PO Mapping

	Strength of CO-PO/PSO Mapping							
	POs						**PSOs**	
	1	**2**	**3**	**4**	**5**	**6**	**1**	**2**
CO1	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**
CO2	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**
CO3	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**

D: **Elective II VLSI Architectures for DSP**

Course Outcomes	Description
CO1	Implement different DSP function using HDL
CO2	Implement DSP function using different VLSI software

List of Experiments:

Unit	Content	CO Mapped
1	Implement analysis of Music using DSP function	**CO1,CO2**
2	Implement Face recognition using DSP faction implement in hardware	**CO1,CO2**
3	Develop robot which work on speech command and implement on FPGA hardware	**CO1,CO2**
4	Implement different function of DSP such as circular convolution, IIR and FIR filter using hardware	**CO1,CO2**
5.	Implement VLIW architecture using FPGA hardware	**CO1,CO2**

	Strength of CO-PO/PSO Mapping							
	PO						**PSO**	
	1	**2**	**3**	**4**	**5**	**6**	**1**	**2**
CO1	3		3	3	-	-	-	-
CO2	3		3	3	-	-	-	-

E.Elective II Advanced IoT Applications

Course Outcomes	Description
CO1	**Implement** different types ofCloud service .
CO2	Implantation of applications of IOT in different services, Cloud computing and Bigdata.

List of Experiments:

Unit	Content	Bloom's Taxonomy Level	CO Mapped
1	Compare different Cloud Computing Service and Deployment Models in terms of their working and implementation.	**4**	**CO1**
2	Bulid and test any one IoT-Based application in Healthcare Devices with the help of node MCU(do not use aurdino)	**4**	**CO 2**
3	Implement a data-Centric Framework for Development and Deployment of Internet of Things Applications in Clouds	**4**	**CO 2**
4	Implement Sustainable Water Supply system with the help of Schematic Development of Big Data Collection using Internet of Things (IoT)	**4**	**CO 2**
5.	Design and Developed IOT system for agriculture application	**5**	**CO 2**

F.VLSI for AI & Neural Network

Course Outcomes:

Course Outcomes	Description After successful completion of the course students will be able to
CO1	Apply basic principles of AI
CO2	Analyze applications of AI techniques in intelligent agents
CO3	Demonstrate in intelligent agents, expert systems, artificial neural networks
CO4	Develop applications in an 'AI language', expert system shell, or data mining

	tool.
CO5	Applying scientific method to models of machine learning.

List of Experiments:

Unit No.	Contents	CO mapped
1	Implement a neural network for any suitable application.	CO3,CO4
2	Implement genetic algorithms for any suitable application.	CO3,CO4
3	Design neural network to identify and control nonlinear systems using MATLAB.	CO4
4	Design and how to supervised and unsupervised artificial neural networks	CO4
5	Data fitting, clustering and pattern recognition using neural network toolbox in MATLAB.	CO5

CO-PO Mapping for Practical

K.K.Wagh Institute of Engineering Education and Research, Nashik
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F. Y. M. Tech.(VLSI and Embedded System)
Pattern 2022 Semester: II
ETC225112: Seminar I

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Practical :04hrs/week	**02**	**Oral: 25Marks** **TermWork: 25Marks**

Prerequisite Courses, if any: Semiconductor Theory, Mathematics

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Implement a minor project based on VLSI and Embedded System.	Applying
CO2	Effectively communicate by delivering presentation on a given topic	Analyzing
CO3	Prepare a detailed seminar report using LATEX.	Applying

COURSE CONTENTS

	Seminar I	**(32hrs)**	**COs Mapped – CO1,CO2,CO3**

Seminar I will be based on a minor project. The topic for the minor project will be based on subjects of the first semester.
The student shall submit the seminar report in standard format, duly certified for satisfactory completion of the work by the concerned guide and head of the Department/Institute.

Text Books

NA

Reference Books

1. Raymund F. Wood, Bibliography and the Seminar, Vol. 9, No. 1 (Summer, 2003)
2. Borden, Iain and Katerina Ruedi Ray. The Dissertation: A Guide for Architecture Students. Third Edition. 2014.
3. Turabian, Kate L. A manual for writers of term papers theses, and dissertations. 7th ed., 2007.
4. John Bowden, Writing A Report, 9th Edition: How to Prepare, Write & Present Really Effective Reports, June 2011.

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F. Y. M. Tech.(VLSI and Embedded System)
Pattern 2022 Semester: I
ETC225113: Software application for professional skill upgradation
(LATEX, Power Point & amp;Excel)

Teaching Scheme:	**Credit Scheme:**	**Examination Scheme:**
Practical :04hrs/week	**02**	**Continuous Assessment: 25Marks** **Oral: 25Marks**

Prerequisite Courses, if any: Microsoft Office

Course Outcomes: On completion of the course, students will be able to–

	Course Outcomes	**Bloom's Level**
CO1	Create different types of documents in Latex	Applying
CO2	Createdifferent types of documents in Powerpoint	Applying
CO3	Create different types of documents in Excel	Applying

COURSE CONTENTS

Unit I	**Introduction to Latex**	**(06hrs)**	**COs Mapped – CO1**

Introduction to LaTeX, its installation, and different IDEs. The learner creates the first document using LaTeX, organizes content into sections using the article and book class of LaTeX.
Styling Pages: Review of different paper sizes, examines packages, format the page by setting margins, customizing header and footer, changing the page orientation, dividing the document into multiple columns.

Unit II	**Formatting Content in Latex**	**(06hrs)**	**COs Mapped - CO1**

This topic concentrates on formatting text (styles, size, alignment), adding colors to text and entire pages, and adding bullets and numbered items. It concludes by explaining the process of writing complex mathematics.

Unit III	**Tables and Images in Latex**	**(06hrs)**	**COs Mapped – CO1**

The topic starts by creating basic tables, adding simple and dashed borders, merging rows and columns, and handling situations where a table exceeds the size of a page. The sessions then continue to add an image, explore different properties like rotate, scale,etc

Unit IV	**PowerPoint**	**(06hrs)**	**COs Mapped – CO2**

Basics of powerpoint, Create Presentations, Insert and modify tables and charts, Insert clipart images and shapes to slides, Work with Graphics and Media, Insert and edit animations and slide transition

Unit V	Microsoft Excel	(06hrs)	COs Mapped – CO3
Create, open and view a workbook, Work with cell references, Learn to use functions and formulas.,Create and edit charts and graphics, Filter and sort table data,Import and export data			

Text Books

1. A. Diller, LaTeX Line by Line, published by Wiley.

Reference Books

1. M. Goossens, F. Mittelbach, and A. Samarin, The LaTeX Companion, published by Addison-Wesley, ISBN 0-201-54199-8
2. N. Walsh, Making TeX Work, published by O'Reilly & Associates, ISBN 1-56592-051-1

Guidelines for Continuous Assessment of Theory Course		
Sr. No.	**Components for Continuous Assessment**	**Marks Allotted**
1	**Assignment:** 1. Create a Latex Report Containing Chapter, Sections, Subsections, Figures (5 Marks) 2. Create a Latex Documents which uses mathematical Equations and Tables (5 Marks) 3. Create a Research Paper document in Latex (5 Marks) 4. Create a Seminar Report in Microsoft Powerpoint (5 Marks) 5. Create an Excel Document which performs following tasks: Create Sheets, Create Tables, Insert Tables & Figures, Use of equations, Use Filters, import and export documents. (5 Marks)	**25**